nuvoTon

W681308

USB AUDIO CONTROLLER

Data Sheet

Revision 1.2

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1. General Description

W681308 USB Audio Controller from Nuvoton integrates fast 8051 Microcontroller Unit (MCU), Universal Serial Bus (USB) 2.0 Full Speed compliant controller with PHY, 16bit high quality Analog to Digital Converter / Digital to Analog Converter (ADC/DAC) with 8/16/48 KHz wide band sampling rates, speaker phone and echo cancellation, 8 KB One Time Programmable (OTP) program memory and 1 KB data memory in a single 48 pin Low-profile Quad Flat Package (LQFP). MCU includes Joint Test Access Group (JTAG) In-Circuit Emulation(ICE) interface and can handle customer programs such as keypad scan, LCD control, caller list download, and USB and CODEC control among other features. W681308 provides highest integration and low BOM cost solution with 8051-based development platform for USB Audio peripherals and USB VoIP devices such as Skype® , other IM and SIP-based application.

With Nuvoton's market proven CODEC product experience, W681308 is designed to provide high audio quality in VoIP and audio devices applications and deliver USB Audio/VoIP solution with the shortest time to market, time to volume and time to profit

2. Features

8 Bit Turbo MCU

- Embedded 12/24/48 MHz Turbo 8051 MCU with 4 Clocks per machine Cycle
- 1 KB system RAM, 8 KB OTP ROM
- 256 byte internal RAM (8051)
- Power on Reset circuit
- Software Idle mode
- In Circuit Emulation (ICE) through JTAG Interface
-

High Quality 16 bit Mono Audio Linear CODEC

- Built-in 8/16/48 KHz sampling rate wideband mono audio CODEC and true 16-bit resolution ADC/DAC with internal 24-bit audio processing for both record and playback
- Analog microphone(MIC) amplifier and speaker driver with internal programmable gain stage
- 82 dB Receive SNR @ 8 Ohm load

USB 2.0 Full speed (FS) Interface with integrated PHY

- USB 2.0 FS compliant device controller and PHY with 12 Mbps communication speed
- Support 6 USB endpoints configuration: Control, ISO IN/OUT, Bulk IN/OUT and Interrupt IN
- 512-Byte RAM-based USB descriptor for multiple USB device support through 8051 MCU
- Less than 500uA supply current in suspend mode
-
- Fully integrated cap-less microphone amplifier with microphone bias
- Dual earphone / speaker driver and buzzer
- Integrated DAC switch for earphone or speaker phone

Integrated Acoustic Echo Cancellation (AEC)

- Support both half-duplex AEC and 32ms full duplex AEC
- Built-in digital Auto Gain Control (AGC) with microphone input for speaker phone application

Integrated keypad control pins and GPIO

- Suitable for VoIP application
- Volume up and down
- Dial / hang up
- Microphone and speaker phone mute
- LED indicators

- Number pad control
- User programmable keys
- Keypad scanning
- LCD Module interface control

UART

- Programmable UART port for serial data application

PCM Interface

- Master linear PCM interface to external PCM device such as Nuvoton's ProX CODEC/SLIC

SPI interface

- Works in master mode to control Liquid Crystal Display (LCD) Module or other SPI slave devices
- Support Winbond serial flash device with SPI interface

W2S 2 Wire interface

- Support 2 wire interface for EEPROM three format page modes

USB 5V voltage supply

- Built-in linear regulator on chip supports 3.3V to 1.8V conversion for digital core power
- USB 5V to 3.3V supply power using external transistors

Package

- 48-pin LQFP package 7mmx7mmx1mm

Application

- USB audio peripheral box/ USB sound card
- USB microphone / USB mono headset
- Wired and Wireless USB VoIP phone with LCD
- USB VoIP ATA and Gateway
- PSTN and USB VoIP dual phone
- General USB MCU and audio application

3. Pin Configuration

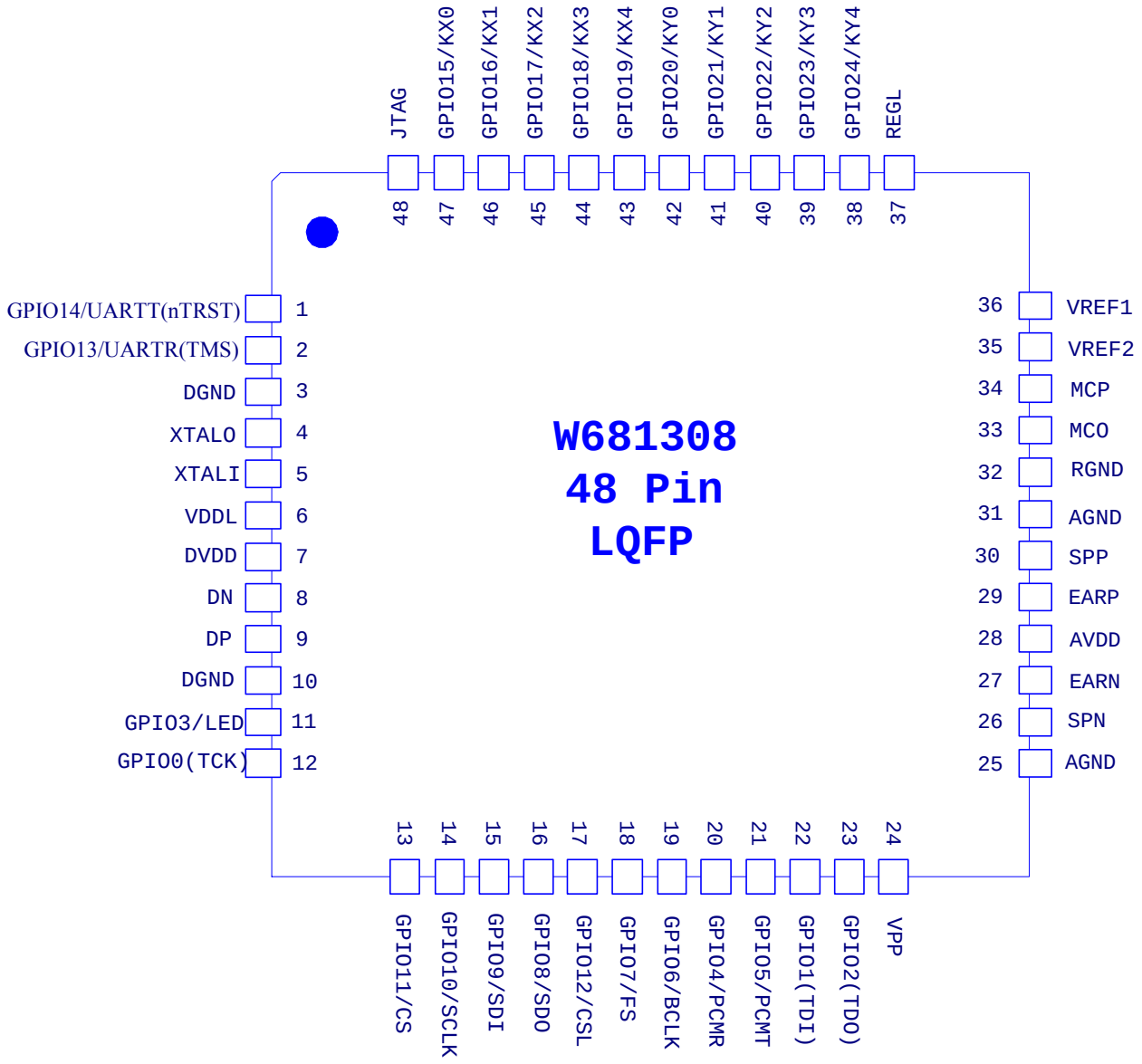


Figure 1 Pin diagram

4. Pin Description

Please refer to Design Guide for product design details.

Pin Name	Pin No	State in Reset	Functionality	Pin Type		Driver Strength
UARTT /nTRST /GPIO 14	1	Pull-H	UART TX data / JTAG TAP controller reset input /GPIO 14	D	I/O	2 mA
UARTR /TMS /GPIO 13	2	Pull-H	UART Rx data / JTAG TMS input / GPIO 13	D	I/O	2 mA
DGND	3		Digital ground supply voltage	D	P	—
XTALO	4		Crystal clock output	A	O	—
XTALI	5		Crystal clock input	A	I	—
VDDL	6		Logic supply voltage	D	P	—
DVDD	7		Digital supply voltage	D	P	—
DN	8		USB D- connection	A	I/O	—
DP	9		USB D+ connection	A	I/O	—
DGND	10		Digital ground supply voltage	D	P	—
LED/GPIO 3	11	Pull-H	LED connection / GPIO 3	D	I/O	16 mA
TCK/GPIO 0	12	Pull-H	JTAG Clock with internal pull up / GPIO 0	D	I/O	16 mA
CS/GPIO 11	13	Pull-H	Chip select (used for SPI flash or normal SPI) /GPIO 11	D	I/O	2 mA
SCLK/GPIO 10	14	Pull-L	Serial port bit clock (For SPI flash or normal SPI) /GPIO 10	D	I/O	2 mA
SDI/GPIO 9	15	Pull-L	Serial port data in (SPI flash/ SPI) /GPIO 9	D	I/O	2 mA
SDO/GPIO 8	16	Pull-H	Serial port data out (SPI flash/ SPI) /GPIO 8	D	I/O	2 mA
CSL/GPIO 12	17	Pull-H	LCD, LCM chip select /GPIO 12	D	I/O	2 mA
FS/GPIO 7	18	Pull-L	PCM Frame Sync output /GPIO 7	D	I/O	2 mA
BCLK/GPIO 6	19	Pull-L	PCM Bit Clock output or input / GPIO 6	D	I/O	2 mA
PCMR/GPIO 4	20	Pull-L	Serial PCM Receive data input / GPIO 4	D	I/O	2 mA
PCMT/GPIO 5	21	Pull-L	Serial PCM Transmit data output / GPIO 5	D	I/O	2 mA
TDI/GPIO 1	22	Pull-H	JTAG Data Input / GPIO 1	D	I/O	2 mA

Pin Name	Pin No	State in Reset	Functionality	Pin Type		Driver Strength
TDO/GPIO 2	23	Pull-L	JTAG Data Output / GPIO 2	D	I/O	2 mA
VPP	24		Reset signal for digital core. Tie this pin to 6.75V for programming the OTP ROM	A	P	—
AGND	25		Analog ground supply voltage	A	P	—
SPN	26		Speaker1 negative connection	A	O	—
EARN	27		Speaker2 negative connection	A	O	—
AVDD	28		Analog supply voltage	A	P	—
EARP	29		Speaker2 positive connection	A	O	—
SPP	30		Speaker1 positive connection	A	O	—
AGND	31		Analog ground supply voltage	A	P	—
RGND	32		Low noise ADC and DAC reference	A	P	—
MCO	33		The microphone amplifier output	A	G	—
MCP	34		Microphone positive connection	A	O	—
VREF2	35		Voltage reference	A	O	—
VREF1	36		Voltage reference	A	O	—
REGL	37		Linear regulator base control output	A	O	—
KY4/GPIO 24	38	Pull-H	Keypad row Y4 connection /GPIO 24	D	I/O	2 mA
KY3/GPIO 23	39	Pull-H	Keypad row Y3 connection /GPIO 23	D	I/O	2 mA
KY2/GPIO 22	40	Pull-H	Keypad row Y2 connection /GPIO 22	D	I/O	2 mA
KY1/GPIO 21	41	Pull-H	Keypad row Y1 connection /GPIO 21	D	I/O	2 mA
KY0/GPIO 20	42	Pull-H	Keypad row Y0 connection /GPIO 20	D	I/O	2 mA
KX4/GPIO 19	43	Pull-L	Keypad column X4 connection /GPIO 19	D	I/O	2 mA
KX3/GPIO 18	44	Pull-L	Keypad column X3 connection /GPIO 18	D	I/O	2 mA
KX2/GPIO 17	45	Pull-L	Keypad column X2 connection /GPIO 17	D	I/O	2 mA
KX1/GPIO 16	46	Pull-L	Keypad column X1 connection /GPIO 16	D	I/O	2 mA
KX0/GPIO 15	47	Pull-L	Keypad column X0 connection /GPIO 15	D	I/O	2 mA
JTAG	48	Pull-L	Tie to DGND for normal operation. Tie to DVDD to enable JTAG function.	D	I	2 mA

Table 1 Pin Description

NOTE: All GPIO pins modes are controlled by register settings.

5. Block Diagram

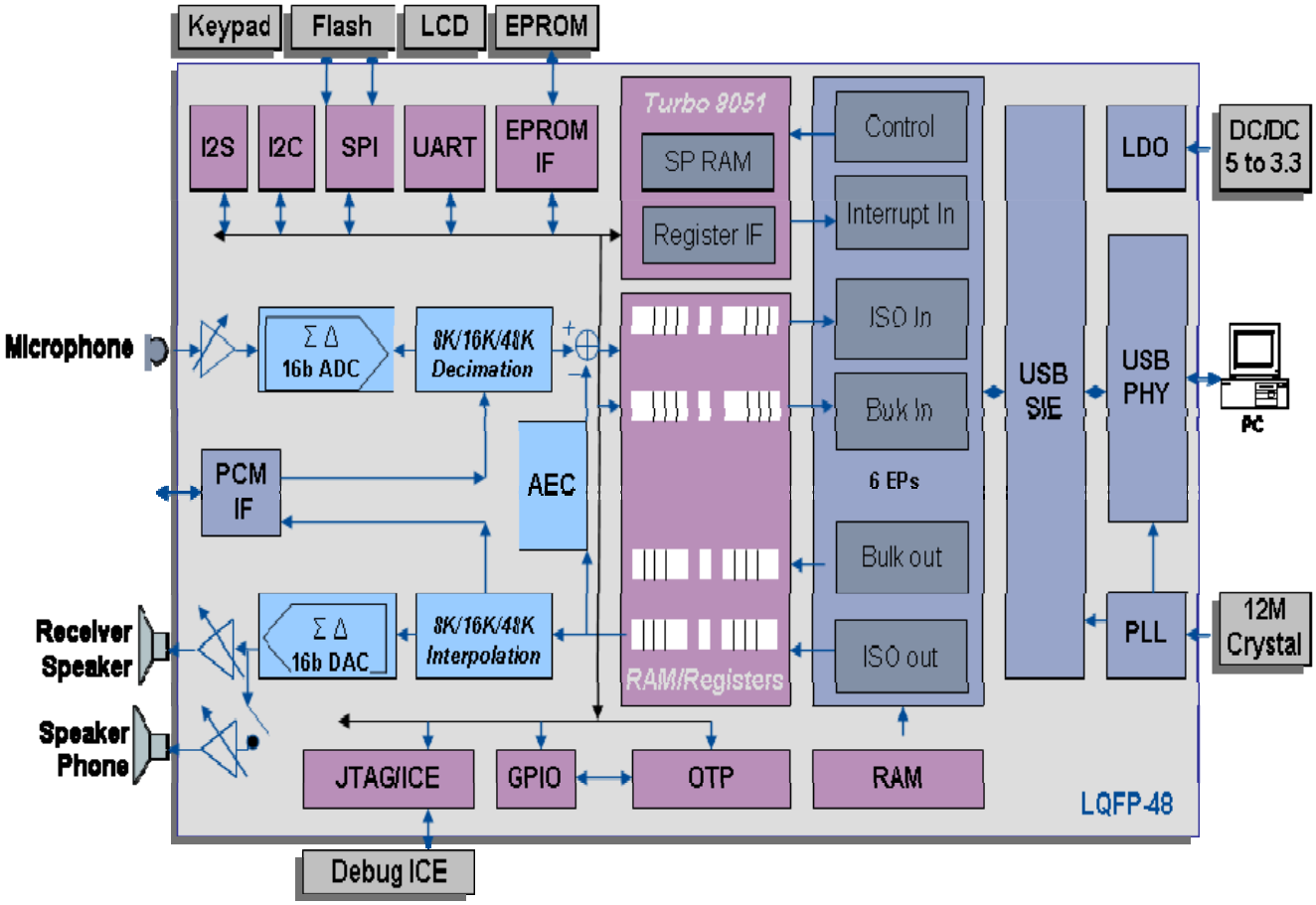


Figure 2 W681308 Function Block Diagram

There are 4 major function block groups in the USB Audio Controller:

- Turbo 8051 MCU, registers, OTP/RAM memory and peripheral ports
- 16-bit audio quality CODEC with AEC/AGC
- USB 2.0 FS interface with SIE, Full Speed PHY and 6 end points
- SPI / UART / I2C / PCM / I2S and GPIO interfaces.

6. Memory Map

6.1 Program Memory map

Memory is mapped into program memory and data memory. Program memory is mapped from 0x0000 to 0x1FFF (8 KB), it is used by internal OTP.

6.2 Data Memory map

Data memory address	Size (Byte)		Function
	Total	Available	
0x1440 ~ 0x1443	4	4	Interrupt Control Registers
0x144A ~ 0x145F	22	20	Keypad IO, LCD, UART and GPIO Control Registers
0x1460 ~ 0x146F	16	16	Gain stage and Mixer Control Registers
0x1470 ~ 0x1474	16	5	PCM Control Registers
0x1480 ~ 0x148A	16	11	CODEC Control Registers
0x14A0 ~ 0x14AF	16	15	SPI Control Registers
0x14B0 ~ 0x14BA	16	11	W2S Control Registers
0x14C0 ~ 0x14C5	16	5	Ring Tone(PWM) Control Registers
0x1600 ~ 0x167F	128	120	Full/Half Duplex AEC Control Registers
0x1680 ~ 0x16FF	128	16	AGC Control Registers
0x1800 ~ 0x19FF	512	57	USB Control Registers
0x2000 ~ 0x23FF	1024	1024	USB RAM Based Descriptor Field
0x2800 ~ 0x2FFF	2048	2048	Full Duplex AEC RAM
0x3000 ~ 0x33FF	1024	1024	System RAM

7. Registers

The registers are mapped by function.

7.1 MCU Clock Rate Select Register

Address	Name	Mode	Value At Reset	Function
0x1440	MCU Rate Select	R/W	0x00	MCU system clock rate selection

7.2 Interrupt Control Registers

Address	Name	Mode	Value At Reset	Function
0x1441	Interrupt Source	R/W	0x00	Enable / Disable Interrupt source
0x1442	Interrupt Enable	R/W	0x00	Enable / Disable Interrupt function
0x1443	Interrupt Priority	R/W	0x00	Set Interrupt priority

7.3 Keypad IO, LCD, UART and GPIO Control Registers

Address	Name	Mode	Value At Reset	Function
0x144A~ 0x144B	GPIO [14:0] Pull Up/Down Control	R/W	0x00	Enable/Disable GPIO [14:0] Pull Up/Down
0x144C~ 0x144F	Keypad I/O (GPIO [24:15]) and GPIO [14:0] Pull Up/Down Selection	R/W	0x00	Select Pull Up/Down for Keypad I/O (GPIO [24:15]) and GPIO [14:0]
0x1450~ 0x1453	Keypad I/O(GPIO [24:15]) and GPIO [14:0] Status	R/W	0x00	Indicate Keypad I/O(GPIO [24:15]) and GPIO [14:0] pin status
0x1454~ 0x1457	Keypad I/O(GPIO [24:15]) and GPIO [14:0 Direction Control	R/W	0x00	Select Keypad I/O(GPIO [24:15]) and GPIO [14:0] Input/Output Direction
0x1458~ 0x145B	Keypad I/O(GPIO [24:15]) and GPIO [14:0] Interrupt control	R/W	0x00	Enable/Disable Keypad I/O(GPIO [24:15]) and GPIO [14:0] Interrupt
0x145E	LCD Control	R/W	0x00	Enable/Disable LCD data, clock and chip selection control.
0x145F	UART I/O Control	R/W	0x00	Enable/Disable UART I/O control.

7.4 Gain Stage and Mixer Control Registers

Address	Name	Mode	Value At Reset	Function
0x1460	Gain Stage and Mixer Control	R/W	0x00	Enable/Disable Gain Stage for Side tone Gain, CODEC to AEC Gain, AEC to CODEC Gain, AEC to Mixer Gain, Mixer to AEC Gain and USB in/USB out Gain. Select Mixer mode for USB, CODEC and PCM.
0x1461~ 0x1467	Gain Stage Index	R/W	0x00	Set Audio Gain Index Register Value (Side tone Gain, CODEC to AEC Gain, AEC to CODEC Gain, AEC to Mixer Gain, Mixer to AEC Gain, USB in and USB out Gain)
0x1468~ 0x146B	MCU Record	R	0x00	Enable/Disable MCU to monitor USB ISO In/Out data
0x146C~ 0x146F	MCU Play	R/W	0x00	Enable/Disable MCU write data to USB and CODEC

7.5 PCM Control Registers

Address	Name	Mode	Value At Reset	Function
0x1470	PCM Control	R/W	0x00	Enable/Disable PCM Interface and Bit Clock / Frame Sync selection
0x1472	PCM Frame Sync Length	R/W	0x00	Set Frame Sync pulse length

7.6 CODEC Control Registers

Address	Name	Mode	Value At Reset	Function
0x1480	CODEC control	R/W	0x00	Enable/Disable CODEC, Select Sampling Rate and High Pass Frequency
0x1481	Dither Control	R/W	0x00	Enable/Disable Dither Function
0x1482~ 0x1483	CODEC ADC Digital Gain	R/W	0x04 0x00	Set Digital ADC Path Gain
0x1484~ 0x1485	CODEC DAC Digital Gain	R/W	0x04 0x00	Set Digital DAC Path Gain
0x1488	CODEC MIC Control	R/W	0x00	Set microphone bias voltage and bias resistor reference
0x1489	CODEC MIC Control	R/W	0x00	Select MIC interface mode and Set microphone gain
0x148A	CODEC Speaker Control	R/W	0x00	Attenuate speaker phone/ earphone speaker and Set speaker gain
0x148B	CODEC Analog Control	R/W	0x00	Enable/Disable CODEC Analog Block

7.7 SPI Control Registers

Address	Name	Mode	Value At Reset	Function
0x14A0	SPI Clock and Interface	R/W	0x00	Enable/Disable SPI interface and Select SPI bit clock rate
0x14A1	SPI Command Interface Control	R/W	0x00	Set SPI interface command length, R/W and other control
0x14A2	SPI Data Length	RW	0x00	Set SPI interface data field length
0x14A3	SPI Interrupt Control	R/W	0x00	Enable/Disable SPI interface interrupt
0x14A4~ 0x14A8	SPI Command Byte Control	RW	0x00	Set SPI interface command byte 1 to 5
0x14AB	SPI Clock Format Control	RW	0x00	Set SPI interface clock format
0x14AC	SPI FIFO Data	RW	0x00	Read/write data from SPI interface FIFO
0x14AD	SPI Byte Count	R	0x00	Current SPI interface FIFO counter value
0x14AE	SPI Write Count	R/W	0x00	MCU current Write point for SPI interface FIFO
0x14AF	SPI Read Count	R/W	0x00	MCU current Read point for SPI interface FIFO

7.8 W2S Control Registers

Address	Name	Mode	Value At Reset	Function
0x14B0	W2S Enable	R/W	0x00	Enable/Disable W2S bus controller
0x14B1	EEPROM control	R/W	0x00	Set different page mode and page size of EEPROM
0x14B2~ 0x14B3	W2S Clock	R/W	0x00	Set W2S bit clock rate
0x14B4	W2S R/W FIFO	R/W	0x00	Read/Write W2S compatible device
0x14B5	W2S R/W Operation Control	R/W	0x00	Set W2S Read/Write and FIFO control
0x14B6	W2S Status	R/W	0x00	Indicate W2S FIFO space and ACK signal status
0x14B7	FIFO Read Pointer	R/W	0x00	Indicate W2S FIFO read pointer
0x14B8	FIFO Write Pointer	R/W	0x00	Indicate W2S FIFO write pointer
0x14B9	ACK Failure Detect	R/W	0x00	Set ACK failure detect and indicate failure data pointer in FIFO
0x14BA	W2S Miscellaneous Control	R/W	0x00	Indicate status for SCL_in, finite state machine state and interrupt signal status

7.9 Ring Tone (PWM) Control Registers

Address	Name	Mode	Value At Reset	Function
0x14C0	PWM Clock	R/W	0x00	Enable/Disable PWM Operation Clock
0x14C2	PWM Tone1 Control	R/W	0x00	Set Tone 1 Volume
0x14C3	PWM Tone1 Frequency	R/W	0x00	Set Tone 1 Frequency
0x14C4	PWM Tone2 Control	R/W	0x00	Set Tone 2 Volume
0x14C5	PWM Tone2 Frequency	R/W	0x00	Set Tone 2 Frequency

7.10 Full/Half Duplex Acoustic Echo Cancellation (AEC) Control Registers

Address	Name	Mode	Value At Reset	Function
0x1600	AEC Configuration	R/W	0x96	Set AEC Configuration parameters
0x1601	AEC Reset Control	R/W	0x08	Set AEC power down and reset function
0x1602	AEC Mode Control	R/W	0x03	Set AEC Full/Half duplex mode and Noise suppressor
0x1605	Double Talk Long Term Power Time Constant	R/W	0x09	Set time constant for long term power estimation of double talk
0x1606	Double Talk Short Term Power Time Constant	R/W	0x0B	Set time constant for short term power estimation of double talk
0x1607~ 0x1608	Double Talk Hangover Time	R/W	0x0020	Set hangover time window of double talk detection algorithm
0x1609~ 0x160A	Double Talk Deviation Threshold	R/W	0x19A8	Set deviation power threshold of double talk
0x160B~ 0x161C	Double Talk Long Term Power Threshold	R/W	0x0000	Set power threshold for long term power estimation of double talk
0X160D~ 0x160E	Double Talk Short Term Power Threshold	R/W	0x1010	Set power threshold for short term power estimation of double talk
0X160F	AEC Divergence Threshold	R	0x0F	Set AEC Divergence threshold
0x1610	Voice Detect Long Term Power Time Constant	R/W	0x09	Set time constant for long term power estimation of Voice Detect
0x1611	Voice Detect Short Term Power Time Constant	R/W	0x0B	Set time constant for short term power estimation of Voice Detect
0x1612~ 0x1613	Voice Detect Hangover Time	R/W	0x0009	Set hangover time window of Voice Detect detection algorithm

Address	Name	Mode	Value At Reset	Function
0x1614~ 0x1615	Voice Detect Deviation Threshold	R/W	0x1998	Set deviation power threshold of Voice Detect
0x1616~ 0x1617	Voice Detect Long Term Power Threshold	R/W	0x1998	Set power threshold for long term power estimation of Voice Detect
0x1618~ 0x1619	Voice Detect Short Term Power Low Threshold	R/W	0x0BA8	Set Low power threshold for short term power estimation of Voice Detect
0X161A~ 0X161B	Voice Detect Short Term Power High Threshold	R/W	0x1038	Set high power threshold for short term power estimation of Voice Detect
0X161C~ 0X161D	Voice Detect Short Term Power Average Threshold	R/W	0x0000	Set average power threshold for short term power estimation of Voice Detect
0X161E~ 0X161F	Power Cut Off Control	R/W	0x1998	Set zero reference bias for power cut off estimation
0x1620~ 0x1621	AGC Threshold	R/W	0x2000	Set maximum output power of AGC
0x1622~ 0x1623	AGC Noise Threshold	R/W	0x0320	Set AGC calculated input power with time constant
0x1624	AGC Gain from AEC	R/W	0x02	Set maximum gain for post echo cancellation signal
0x1625	AGC Gain Time constant	R/W	0xBB	Set delay time constant for long term gain estimation
0x1626	AGC Gain Time constant	R/W	0x09	Set delay time constant for short term gain estimation
0x1628	Soft Clip Control	R/W	0x00	Enable/Disable soft clip(SC) function
0x1629	Soft Clip Normal Gain Index	R/W	0x00	Set gain index of voice detect for soft clip module at normal gain mode
0x162A	Soft Clip Low Gain Index	R/W	0x00	Set gain index of voice detect for soft clip module at low gain mode
0x162B~ 0x162C	Soft Clip Threshold	R/W	0x1000	Set threshold level to select soft clip gain mode
0x162D	Soft Clip Power Time Constant	R/W	0x07	Set time constant for short term power calculation of voice detect soft clip
0x162E	Soft Clip Gain Time Constant	R/W	0x07	Set time constant to smooth gain mode change of soft clip
0x1630	Acoustic Suppression 1 Time Constant	R/W	0x77	Set time constant of acoustic suppression (AS1) for convergence towards target
0x1631- 0x1632	Acoustic Suppression 1 attenuation	R/W	0x1CA8	Set maximum attenuation value for acoustic suppression (AS1) algorithm
0x1633	Acoustic Suppression 2 Time Constant	R/W	0x77	Set time constant of acoustic suppression (AS2) for convergence towards target
0x1634~ 0x1635	Acoustic Suppression 2 attenuation	R/W	0x1CA8	Set maximum attenuation value for acoustic suppression (AS2) algorithm
0x1638	Noise Suppressor Control	R/W	0xBB	Set noise suppressor gain index and short term power time constant
0x1639	Noise Suppressor Gain Time Constant	R/W	0xBB	Set time constant for rise and fall of noise suppressor gain index

Address	Name	Mode	Value At Reset	Function
0x163A~ 0X163B	Noise Suppressor Active Power Threshold	R/W	0x03E8	Set threshold level for active noise suppressor
0x1640~ 0x1641	Short Term Power voice detector	R	0x0000	Indicate Short Term Power calculated by the voice detector (VD).
0x1642~ 0x1643	Long Term Power Voice Detector	R	0x0000	Indicate Long Term Power calculated by the voice detector (VD).
0x1644~ 0x1645	Voice Detector Power Deviation	R	0x0000	Indicate Power Deviation estimated by the voice detector (VD).
0x1648~ 0x1649	Short Term Power Double Talk	R	0x0000	Indicate Short Term Power calculated by double-talk detector (DT).
0x164A~0x 164B	Long Term Power Double Talk	R	0x0000	Indicate Long Term Power calculated by double-talk detector (DT).
0x164C~0x 164D	Double Talk Power Deviation	R	0x0000	Indicate Power Deviation estimated by the double-talk detector (DT).
0x1680	AGC Control	R/W	0x00	Enable / Disable AGC and Set max gain control
0x1681	AGC Initial Gain Control	R/W	0x00	Enable/Disable AGC initial gain setting
0x1682	AGC Gain Time	R/W	0x00	Set decreasing and increasing gain time for AGC
0x1683	AGC Peak Release Time	R/W	0x00	Set release time for AGC peak voice level
0x1684	AGC Gain Monitor	R	0x00	Indicate AGC gain status
0x1685	AGC Gain Region Monitor	R	0x00	Indicate AGC gain status at increasing, target or decreasing region.
0x1687~ 0x1689	AGC Short Term Power	R	0x0000	Indicate AGC Short Term Power estimation
0x168A~0x 168B	AGC Target Threshold	R/W	0x0000	Set AGC target region threshold
0x168C~0x 168D	AGC Noise Low Threshold	R/W	0x0000	Set AGC Noise low threshold level
0x168E~0x 168F	AGC Noise High Threshold	R/W	0x0000	Set AGC Noise high threshold level

7.11 USB Controller Registers

Address	Name	Mode	Value At Reset	Function
0x1800	USB Enable	R/W	0x00	Enable/Disable USB 1.1 function control
0x1801~ 0x1803	USB Interrupt Register A	R/W	0x00	Set USB endpoints interrupt enable, status and clear.
0x1804 ~ 0x1806	USB Interrupt Register B	R/W	0x00	Set USB endpoints interrupt enable, status and clear.

Address	Name	Mode	Value At Reset	Function
0x1807 ~ 0x1809	USB Interrupt Register C	R/W	0x00	Set USB Audio Class interrupt enable, status and clear.
0x1810	Endpoint 0 – Control In/Out	R/W	0x00	Set USB Control in/out Endpoint control
0x1811	Control In Data	R/W	0x00	Control in Endpoint Data. Internal FIFO has 1 byte for Control In transmission. If the 3rd Token byte is not equal to 0x01 or 0x03 (HID set report application), this byte will be transmitted instead of Control-IN FIFO and Interrupt-IN FIFO content.
0x1828 ~ 0x182F	Control Out Data	R	0x00	Control Out Endpoint receiving data.
0x1830	Endpoint 1 and 2 – ISO In/Out	R/W	0x00	Set ISO In/Out Endpoint control register.
0x1831	Sampling Frequency	R	0x00	Indicate ISO Sampling Frequency
0x1832-0x1833	Record Volume	R	0x00	Indicate Current Record Volume
0x1834-0x1835	Play Volume	R	0x00	Indicate Current Play Volume
0x1836	HID Control Out Information	R	0x00	Indicate First Packet and Valid Length
0x1837	Max Volume	R	0x00	Indicate Audio Path Max Volume Gain
0x1838	HID Token Information	R/W	0x00	Set HID Token 3rd byte
0x1839	HID Descriptor Length	R/W	0x00	This register value must be equal to the USB descriptor with respect to the HID return length
0x1840 ~ 0x1847	ISO SYNC Speed	R/W	0x00	Set ISO SYNC speed tuning parameter register.
0x1848	Endpoint 3 – Bulk In Control Register	R/W	0x00	Set Bulk In Endpoint control register
0x1849	Bulk In Data	W	0x00	Set Bulk In transmission data register except final data.
0x184A	Bulk In Final Data	W	0x00	Set Bulk In transmission final data register.
0x184B	Bulk In FIFO Empty Flag	R	0x00	Indicate Bulk In transmission data FIFO empty flag.
0x1850	Endpoint 4 – Bulk Out Control Register	R/W	0x00	Set Bulk Out Endpoint control register

Address	Name	Mode	Value At Reset	Function
0x1851	Bulk Out FIFO Length	R	0x00	Indicate Bulk Out Endpoint receiving data FIFO length.
0x1852	Bulk Out Data	R	0x00	Bulk Out Endpoint receiving data FIFO.
0x1858	Endpoint 5 – Interrupt In Control Register	R/W	0x00	Set Interrupt In Endpoint control register
0x1859	USB Interrupt Data Length	R/W	0x00	Interrupt In Endpoint transmission data length
0x1880	USB ISO MCU Enable	R/W	0x00	Enable ISO IN/OUT FIFO access by MCU
0x1881	USB ISO IN FIFO Depth	R	0x00	ISO OUT FIFO depth indication
0x1882	USB ISO OUT FIFO Depth	R	0x00	ISO IN FIFO depth indication
0x1883~ 0x1884	USB ISO IN DATA	R/W	0x00	ISO IN data sample will be written by MCU
0x1885~ 0x1886	USB ISO OUT DATA	R	0x00	ISO IN data sample will be read by MCU
0x2000- 0x21FF	USB Descriptor RAM data filed	R/W	0x00	USB Descriptor
0x2200- 0x223F	HID Control-IN data field	R/W	0x00	HID Control-IN data field
0x2240- 0x227F	HID Interrupt-IN data field	R/W	0x00	HID Interrupt-IN data field
0x2300- 0x233F	HID Control-OUT data field	R/W	0x00	HID Control-OUT data field

8. Microcontroller

8.1 Features

- 8-bit Turbo 8051 Microcontroller with 12/24/48 MHz speed
- 256 bytes of on chip internal data RAM and 1K bytes external data RAM
- Instruction set compatible with Nuvoton Turbo 8051
- Three 8-bit I/O ports
- Three 16-bit timers
- One Full-duplex serial port
- On-Chip debugger via JTAG (Joint Test Access Group) port
- 7 interrupt sources with two level priorities
- Programmable Watchdog Timer
- Two 16-bit data pointers
- On Chip 8 KB OTP (One time programmable) memory

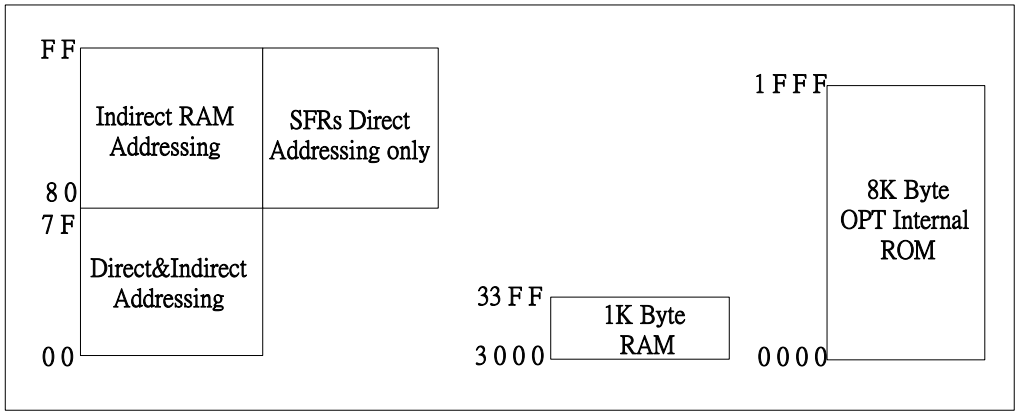
8.2 Memory Organization

8.2.1 Program Memory

On-chip 8k OTP Memory:
All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

8.2.2 Data Memory

The MCU can access 1K bytes of external Data Memory. This memory region is accessed by the MOVX instruction. Additionally it has 256 bytes on chip RAM which can be accessed either by direct addressing or by indirect addressing. Some Special Function Registers (SFRs) can only be accessed by direct addressing.



8.2.3 Special Function Registers (SFR)

Address	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
F8	EIP							
F0	B							
E8	EIE							
E0	ACC							
D8	WDCON							
D0	PSW							
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		
C0					PMR	STATUS		TA
B8	IP	SADEN						
B0	P3							
A8	IE	SADDR						
A0	P2	XRAMAH						
98	SCON	SBUF						
90	P1							
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON

Table 2 W681308 MCU SFR location

8.3 Power Management

The W681308 has IDLE mode operation features that manage and save power consumption of the device.

Enable IDLE mode

The user can set the device into idle mode by writing 1 to the PCON bit of SFR. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the MCU is halted but not to the Interrupt, Timer, Watchdog timer, and Serial ports blocks. This forces the MCU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The ALE and PSEN pins are held high during the idle state. The port pins hold the logical states they had at the time Idle was activated.

The Idle mode can be terminated in two ways:

- **Activation of any enabled interrupt**

Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into idle mode.

- **Activation of reset**

The Idle mode can also be exited by activating the reset. The device can be put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the W681308 is exiting from an idle mode with a reset, the instruction following the one which put the device into idle mode is not executed. So there is no danger of unexpected writes.

8.4 Reset Conditions

There are two ways to put device into reset state: external reset and watchdog reset.

8.4.1 External Reset

The device continuously samples the RST pin at state C4 of every machine cycle. Therefore the RST pin must be held for at least 2 machine cycles to ensure detection of a valid RST high. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is synchronous operation and requires the clock to be running to cause an external reset. Once the device is in reset condition, it will remain so long as RST is 1. Even after RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h.

8.4.2 Watchdog Reset

The Watchdog timer is a free-running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag is set. If the Watchdog reset is enabled and the watchdog timer is not cleared, then 512 clocks from the flag being set, the watchdog timer will generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h.

8.5 Interrupts

The W681308 MCU has three priority levels interrupt structure with 7 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. Additionally, all the interrupts can be globally enabled or disabled.

Source	Flag	Priority	Vector address
External Interrupt 0	IE0	1 (highest)	0003h
Timer 0 Overflow	TF0	2	000Bh
External Interrupt 1	IE1	3	0013h
Timer 1 Overflow	TF1	4	001Bh
Serial Port	RI + TI	5	0023h
Timer 2 Overflow	TF2 + EXF2	6	002Bh
Watchdog Timer	WDIF	7 (lowest)	0063h

Table 3 Interrupt Priority Structure

8.6 Programming Timers and Counters

The MCU of W681308 has three 16-bit programmable timers/counters and one programmable Watchdog timer. The Watchdog timer is operationally quite different from the other three timers.

8.6.1 Timers/Counters 0 and 1

Timer 0 (TM0) and Timer 1 (TM1) are 16-bit Timer/Counters and are nearly identical. Each of these Timers/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two timers can be configured to operate either as timers to count machine cycles or as counters counting external inputs.

In Timer mode, the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock.

In Counter mode, the register is incremented on the falling edge of the corresponding external input pins, T0 for Timer 0 and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the minimum period at which counting will take place is double of the machine cycle.

In either the Timer or Counter mode, the count register will be updated at C3. Therefore, in the Timer mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The Timer or Counter function is selected by the C/T bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own. Bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1.

89H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0
88H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 4 Timer Mode/Control TMOD/TCON SFR

8.6.2 Timer/Counter 2

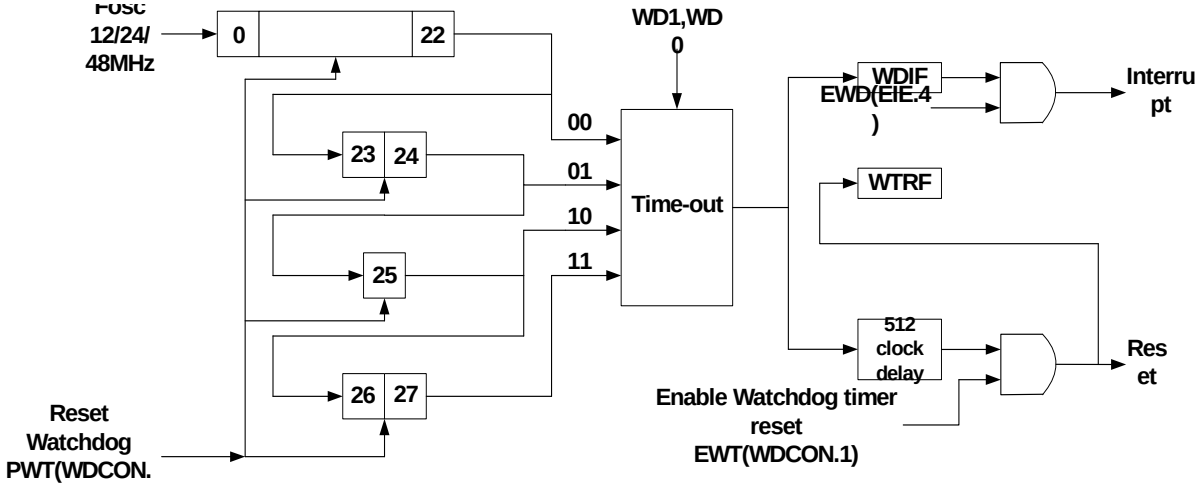
Timer/Counter 2 is a 16 bit up/down counter which is configured by the T2MOD register and controlled by the T2CON register. Timer/Counter 2 is equipped with a capture/reload capability. As with the Timer 0 and Timer 1 counters, they provide wide selection and control of the clock and selection of the operating modes. The clock source for Timer/ Counter 2 can be selected for the crystal oscillator, which is divided by 12 or 4 (C/T2 = 0). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

C9H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2MOD	-	-	-	-	T2CR	-	-	DCEN
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Table 5 Timer 2 Mode/Control TMOD/TCON SFR

8.6.3 Watchdog Timer

The Watchdog timer is a free-running timer that can be programmed by the user to serve as a system supervisor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs the flag WDIF is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the software employed.



When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the RWT allows software to restart the timer. The Watchdog timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the watchdog timer which will allow the code to run without any watchdog timer interrupts. Now the watchdog timer reset is enabled and the watchdog interrupt may be disabled. If any errant code is executed now, then the reset watchdog timer instructions will not be executed at the required instants and watchdog reset will occur.

WD1	WD0	Watchdog Interval	Number of Clocks	Time@12MHz	Time@24MHz	Time@48MHz
0	0	2^{23}	8388608	699.05 ms	349.53 ms	174.76 ms
0	1	2^{25}	33554462	2796.20 ms	1398.10 ms	699.05 ms
1	0	2^{26}	67108864	5592.41 ms	2796.20 ms	1398.10 ms
1	1	2^{28}	268435456	22369.62 ms	11184.81 ms	5592.41 ms

Table 6 Time-Out Values For Watchdog Timer

The Watchdog timer will be disabled by a power-on/fail reset. The Watchdog timer reset does not disable the watchdog timer, but will restart it.

NOTE: In general, software should restart the timer to put it into a known state.

D8H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDCON	-	POR	-	-	WDIF	WTRF	EWT	RWT
External Reset	0	x	0	x	0	x	x	0

Table 7 Watchdog Control WDCON SFR

Control Bit	Name	Function
POR	Power-on Reset Flag	Hardware will set this flag on a power up condition. This flag can be read or written by software. A write by software is the only way to clear this bit once it is set.
WDIF	Watchdog Timer Interrupt Flag	This bit is set by hardware to indicate that the time-out period has elapsed and invoke watch dog timer interrupt if enabled(EWDI=1). This bit must be cleared by software.
WTRF	Watchdog Timer Reset Flag	Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the watchdog timer will have no affect on this bit.

Control Bit	Name	Function
EWT	Enable Watchdog timer Reset	Setting this bit will enable the Watchdog timer Reset function.
RWT	Reset Watchdog Timer	This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWT before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWT is set. This bit is self-clearing.

Table 8 Watchdog Control Bits

WTRF is set to a 1 on a Watchdog timer reset, set to 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is cleared to 0 on a Power-on reset and unaffected by other resets.

To prevent software from accidentally enabling or disabling the watch dog reset function, the bit of WDCON requires Time Access (TA) procedure to write.
Example:

```
mov TA, #0AAH
mov TA, #055H
clr  WDIF
```

WD1, WD0 are Time-out bits for Watchdog Timer located at CKCON.7 and CKCON.6. These bits determine the time-out period of the watchdog timer. The reset time-out period is 512 clocks longer than the watchdog time-out.

WD1	WD0	Interrupt time-out	Reset time-out
0	0	2^{23}	2^{23} + 512
0	1	2^{25}	2^{25} + 512
1	0	2^{26}	2^{26} + 512
1	1	2^{28}	2^{28} + 512

Table 9 Watchdog Timer Timeout Control

8.7 Serial Port (UART)

The MCU serial port is a full-duplex port, and the MCU provides additional features, such as Frame Error Detection and Automatic Address Recognition. The serial port is capable of synchronous and asynchronous communication. In synchronous mode, the MCU generates the clock and operates in half-duplex mode. In asynchronous mode, the serial port can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF, but any write to SBUF writes to the transmit register while any read from SBUF reads from the receive buffer. The serial port can operate in four modes: MOD 0, MOD 1, MOD 2 and MOD 3.

98H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Table 10 Serial Control SCON SFR

8.8 OTP ROM

The W681308 internal OTP ROM is designed to store all application firmware.

- **8kB One-Time Programmable Logic Device**

The OTP programming is done by the injection of hot electrons which are generated by avalanche impact ionization in the bit cell. User can enter JTAG mode to program 8k OTP ROM through JTAG interface pins and signal of PCMT pin will go high simultaneously. The signal of pin PCMT can be used to control external hardware device to apply 6.75V or 3.3V to programming voltage pin VPP. The cells are initialized by ultraviolet light through internal photoemission from the floating gate.

- **Enable OTP Read Protection**

You can write zero to bit 7 of OTP address 0x1fff to turn on the read protection feature.

9. Clock Control and Reset

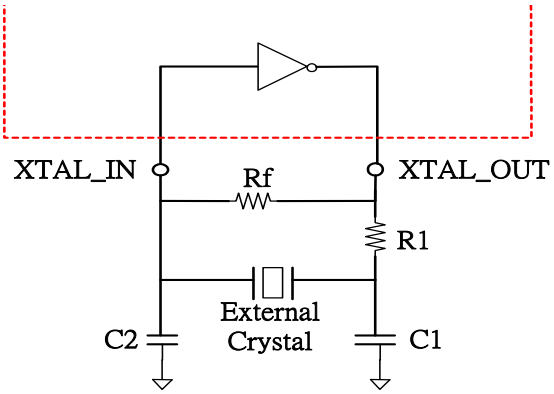
9.1 Clock Control

9.1.1 Overview

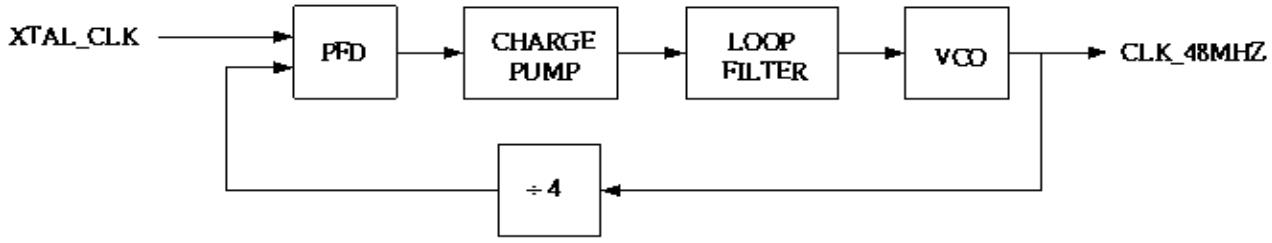
Each register in the 12/24/48 MHz USB Audio Controller is reset synchronously. The Reset and Clock Control function ensures that the system reset signal is correctly generated. The system reset signal is also used to ensure that bi-directional signals are all set to input during initialization.

9.1.2 Clock Generation

The crystal oscillator circuit and the external attachment of a 12 MHz quartz crystal or ceramic resonator is shown below. The Rf is used to DC bias the internal amplifier to operate in the linear region. The R1, C1, and C2 are chosen so as not to overdrive the crystal and to suppress oscillation at higher harmonics. Rf = 1MΩ, R1=270Ω, C1 and C2 are to be 33pf each.



The PLL block diagram is shown below. The PLL uses the output of the crystal oscillator as its reference clock and generate a 48 MHz clock.



9.1.3 Control Register

MCU Rate Select

Address	Access Mode	Value At Reset
0x1440	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MCU Rate Select [7:6]		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

MCU Rate Select [7:6]

MCU Clock Rate select (default = 00)
00 = 12 MHz , Use for CODEC/AEC/USB Controller
01 = 24 MHz
10 = 48 MHz , Use for MCU/USB PHY/Peripherals
11 = Reserved

10. Interrupt Control

10.1 Overview

The W681308 generates internal events, these interrupt events are triggered by the interrupt control logic. The MCU supports two priority levels of interrupts with 6 interrupt sources.

10.2 Functionality

The External Interrupts INT0 and INT1 can be either edge triggered or level triggered,
The Interface and Support logic generate the following interrupts:

- NFS interrupt
- Keypad-Wakeup Interrupt
- GPIO interrupt
- SPI interrupt
- W2S interrupt
- USB interrupt

Three registers control the generation of interrupts in the W681308, the interrupt source register, the interrupt enable register and the interrupt priority register. Each interrupt has a corresponding bit in these three registers.

The interrupt source register is set when an interrupt event occurs and is cleared by MCU.
When the MCU writes to interrupt source, any bit that is set to 1 cause the corresponding bit of interrupt source to be cleared, bits set to 0 are not affected (write “one” to clear).

An Interrupt is generated when (interrupt source) & (interrupt enable) =1 for any of the interrupt sources. For each bit; if interrupt priority = 0, the interrupt is issued to INT0, if interrupt priority = 1, the interrupt is issued to INT1.

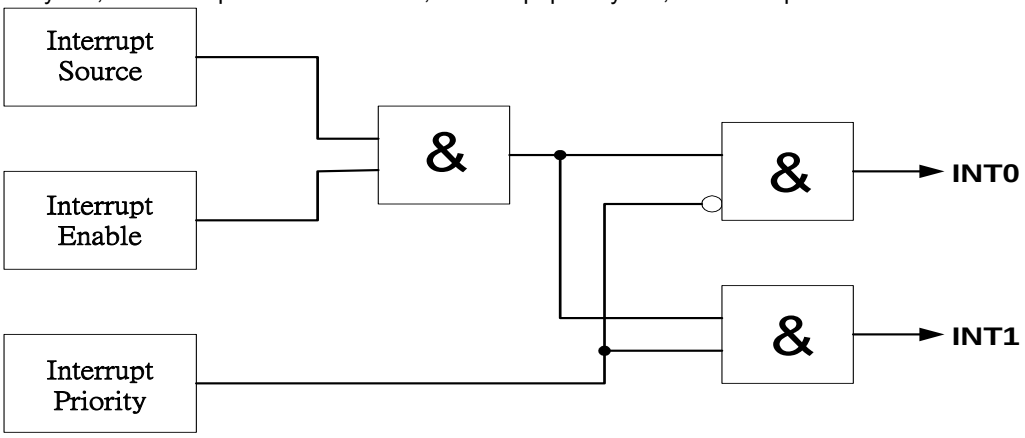


Figure 3 Interrupt Structure

10.3 Interrupt Control Registers

Address	Access Mode	Value At Reset
0x1441 ~ 0x1443	R/W	0x00

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1441	USB Interrupt	W2S Interrupt	SPI Interrupt	GPIO Interrupt	Keypad-Wakeup Interrupt	NFS Interrupt	Reserved	Reserved

NOTE: The NFS interrupt occurs for every 8 CODEC frames.

Interrupt Source Register (0x1441)	Read: 1 = Interrupt 0 = No Interrupt Write: 1 = Clear
Interrupt Enable Register (0x1442)	1 = Enable 0 = Disable
Interrupt Priority Register (0x1443)	0 = INT0 1 = INT1

11. Interface Logic

The W681308 Interface logic consists of:

- Keypad Scanner Interface
- Input/Output GPIO Ports
- LCD/LCM interface
- UART interface
- JTAG Interface
- PCM Interface
- SPI for Serial Data Flash
- W2S Interface

Keypad scanner, GPIO, LCD/LCM and UART interfaces are covered in this section.

11.1 Software Keypad Scanner

The keypads consist of a number of buttons, connected in a row/column arrangement as shown in Figure 4 The default pin KX[4:0] is pull-L and pin KY[4:0] is pull-H, User can follow below steps to scan the keypad by software:

1. Program KX[4:0] pin to output direction and output data 0. Program KY[4:0] pins to input direction.
2. While key is pressed, MCU will be informed by GPIO interrupt then to check KX[4:0] and KY[4:0] status.
3. KX[4:0] keep output data 0, then to read KY[4:0] status by register 0x1451[4:0], By reading KY[4:0] status, MCU can know which bit equal 0, allowing it to determine which row is pressed.
4. Change pin KY[4:0] from input direction to output direction and output data 1. Change pin KX[4:0] from output direction to input direction then to read KX[4:0] status by register 0x1450[4:0]. By reading KX[4:0] status, MCU can know which bit equal 1, allowing it to determine which column is pressed.
5. MCU knows which row and column are pressed, so it can determine which key is pressed.

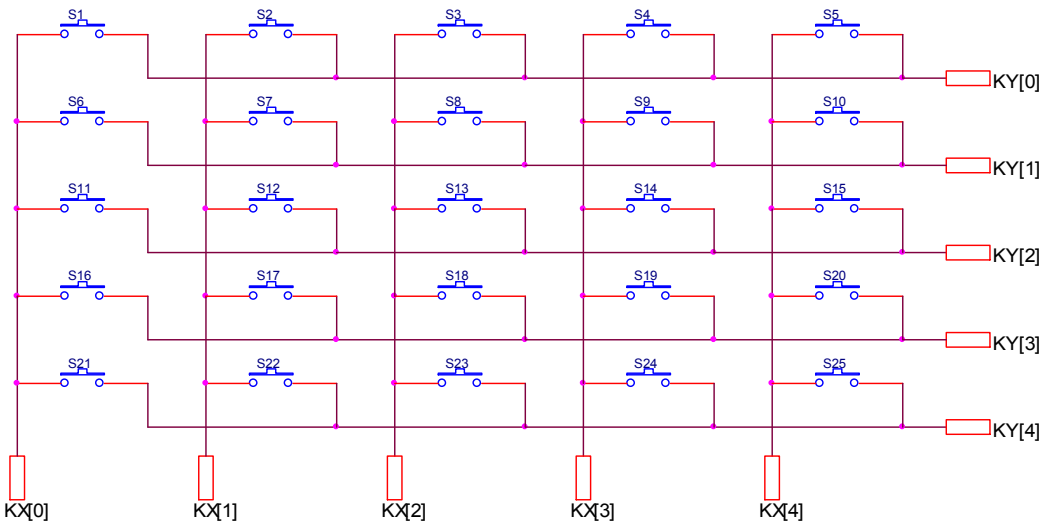


Figure 4 Keypad Scanning Application Circuit

11.2 GPIO s

W681308 has 25 GPIO pins that are mainly used for keypad scanner, LCM controller, SPI, W2S, PCM interface, UART port, JTAG interface and GPIO s.

NOTE: The pin function for LED, CS, SCLK, SDI, SDO and CSL will act as different functions according to the setting of LCD_ENB (0x145E), SPI_ENB (0x14A0), RDY_ENB(0x14AB) and W2S_ENB(0x14B0).

Address	Name	Values					
0x145E[3]	LCD_ENB	0	1	1	0	0	0
0x14A0[7]	SPI_ENB	0	0	1	1	1	0
0x14AB[5]	RDY_ENB	0	0	0	0	1	0
0x14B0[7]	W2S_ENB	0	0	0	0	0	1

Pin Number	Pin Name	Functions					
		GPIO	0x145E[2:0] for LCD driver Control	SPI for LCD driver	SPI for data flash	ISD15000	W2S
11	LED	GPIO 3	GPIO 03	GPIO 3	GPIO 3	SPI_RDY	GPIO 3
13	CS	GPIO 11	GPIO 11	SPI_CS	SPI_CS	SPI_CS	GPIO 11
14	SCLK	GPIO 10	LCD_CKN (0x145E[B1])	SPI_CLK	SPI_CLK	SPI_CLK	W2S_SCL
15	SDI	GPIO 9	GPIO 09	GPIO 9	SPI_SDI	SPI_SDI	GPIO 9
16	SDO	GPIO 8	LCD_TX (0x145E[B0])	SPI_DO	SPI_SDO	SPI_SDO	W2S_SDA
17	CSL	GPIO 12	LCD_CSN (0x145E[B2])	Pull High	GPIO 12	GPIO 12	GPIO 12

11.3 LCD Control

Address	Access Mode	Value At Reset
0x145E	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	LCD_ENB	LCD_CSN	LCD_CKN	LCD_TX

LCD_TX	LCD Write Out Data
LCD_CKN	LCD Write Out Clock
LCD_CSN	LCD Write Out Chip Select Enable (active low)
LCD_ENB	LCD I/O Enable Control : 1 = Enable, 0 = Disable Set this bit to enable LCD control interface : Pin 17 CSL = LCD_CSN Pin 14 SCLK = LCD_CKN Pin 16 SDO = LCD_TX

11.4 UART I/O Control

Address	Access Mode	Value At Reset
0x145F	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UART IO ENB	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

UART IO ENB	UART I/O Enable Control, 1 = Enable, 0 = Disable

12. PCM Interface , Gain Stage and Mixer

12.1 PCM Interface

The PCM module is a 16-bit parallel/serial data transfer interface. It transfers the 16 bits data from Gain-Stage/Mixer to single bit Output, and transfers the one bit signal data of Input pin to 16 bits data buffer to the Gain-Stage / Mixer. In normal operation, the FS and BCLK are generated from the analog PLL module.

PCM Interface specification:

- Master Mode Only
- Support TX / RX path mute
- 8 PCM Bit Clock frequency : 128K, 256K, 512K, 768K, 1M, 1.536M, 2M, 4M Hz.
- 3 frequency selection of the PCM Frame Sync (FS) : 8K, 16K and 48K Hz.
- 16 bit length selection of the PCM Frame Sync (FS) : 1~ 16 bits.
- 4 selection of PCM FS/DATA location + 1 half bit clock delay.
- PCM_FS & PCM_BCLK inverse mode for I2S interface.

12.2 Gain stage

There are 6 programmable gain stages for transmit and receive path. These gain stages are implemented to provide a range of +24 dB to –31.5 dB with 0.5 dB per step. The Figure 5 is shown the location of these digital gain stages. There are 2 side tone paths to select from: One before AEC block, one after AEC block. Side tone gain stage is from -0.5dB to -31.5dB with 0.5dB step.

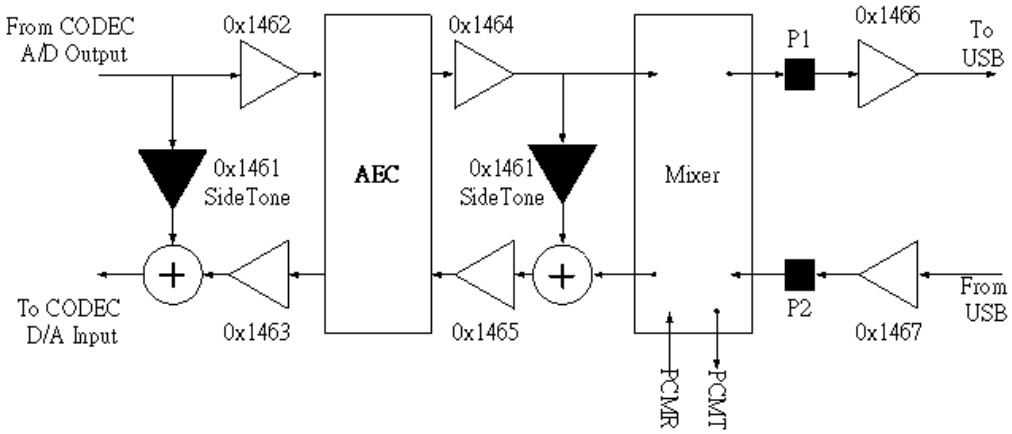


Figure 5 PCM Interface, Gain Stage and Mixer Location

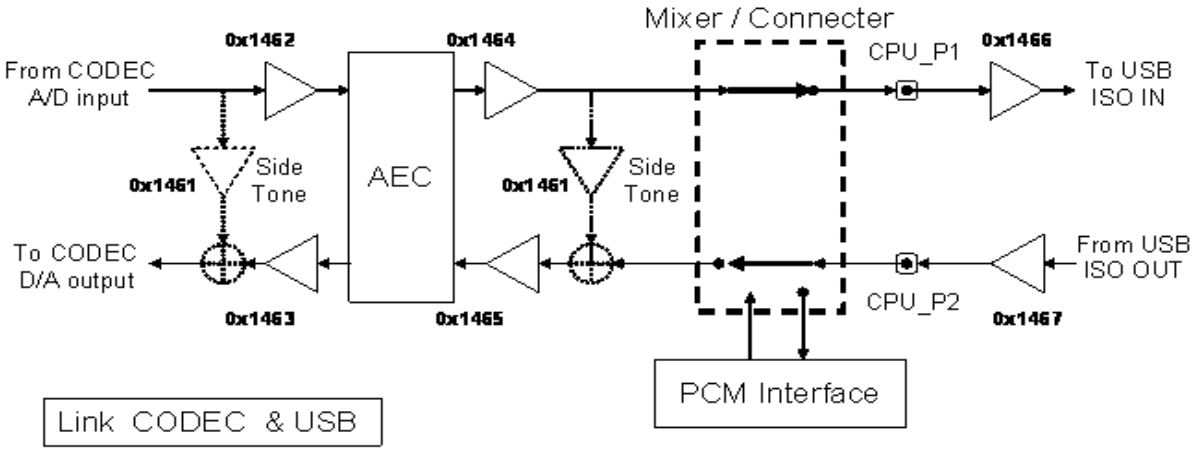
12.3 Mixer

The mixer provides flexible connections among CODEC block, PCM interface and USB block. We will describe each connection case of mixer modes and how to configure them below.

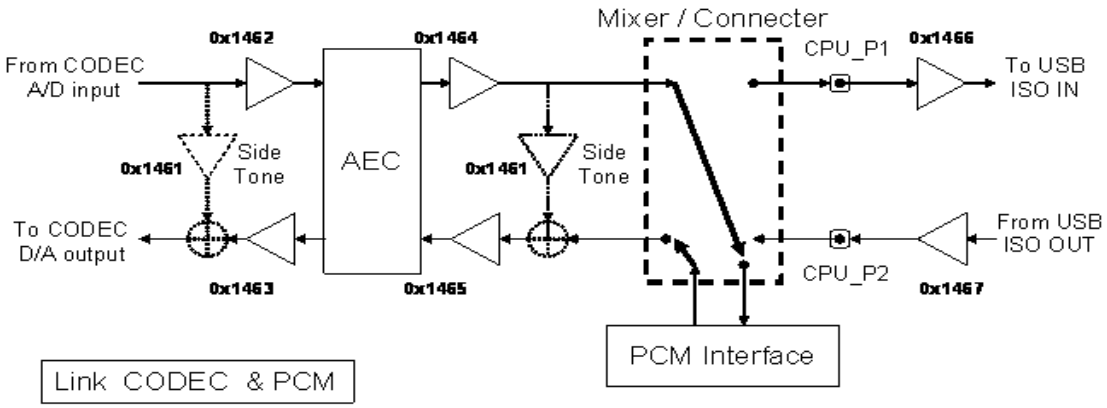
12.4 Connection Case Example

Figure 6 Mixer Connection Case Examples

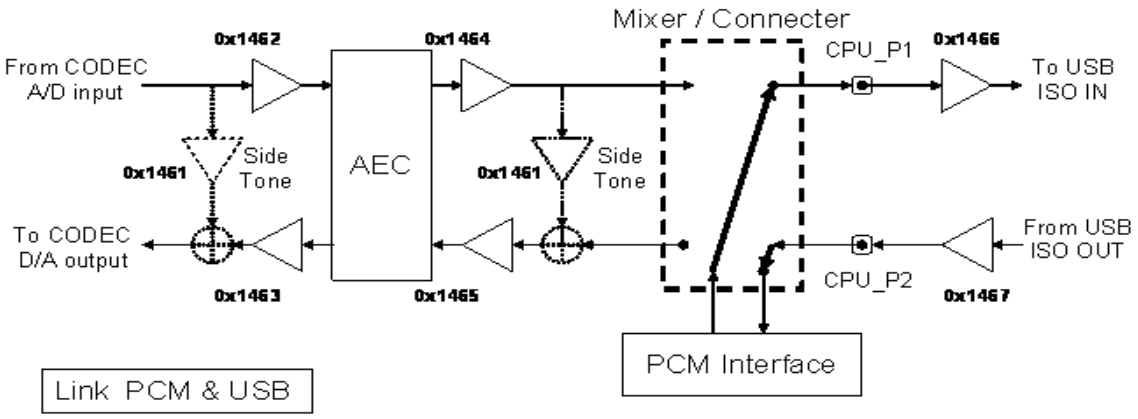
Case 0: Link CODEC and USB



Case 1: Link CODEC and PCM

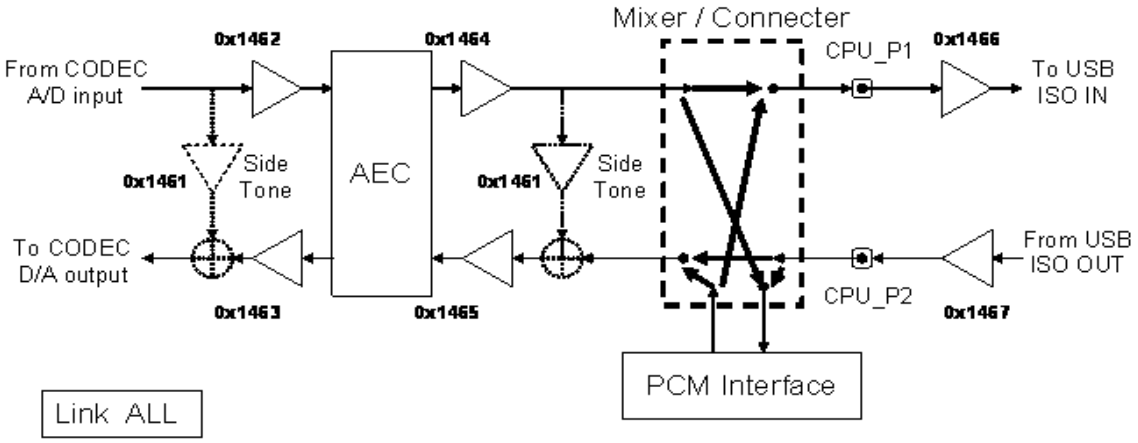


Case 2: Link PCM and USB



Case 3: Link All

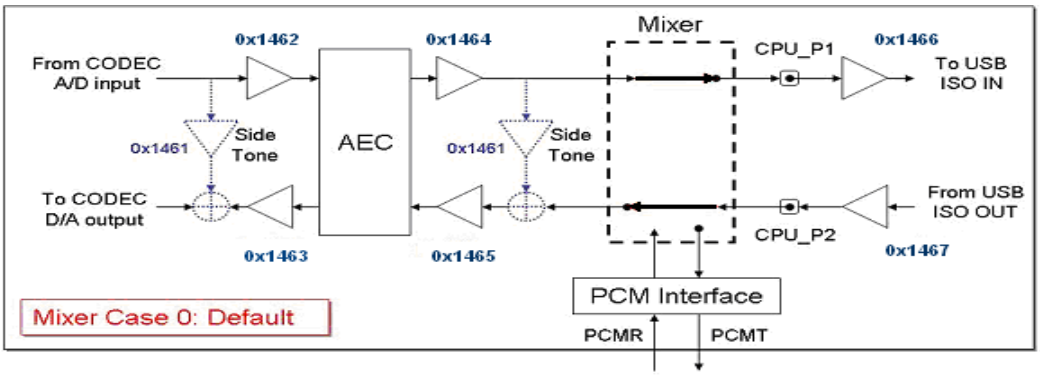
12.5



Mixer Case Examples with Register Setting

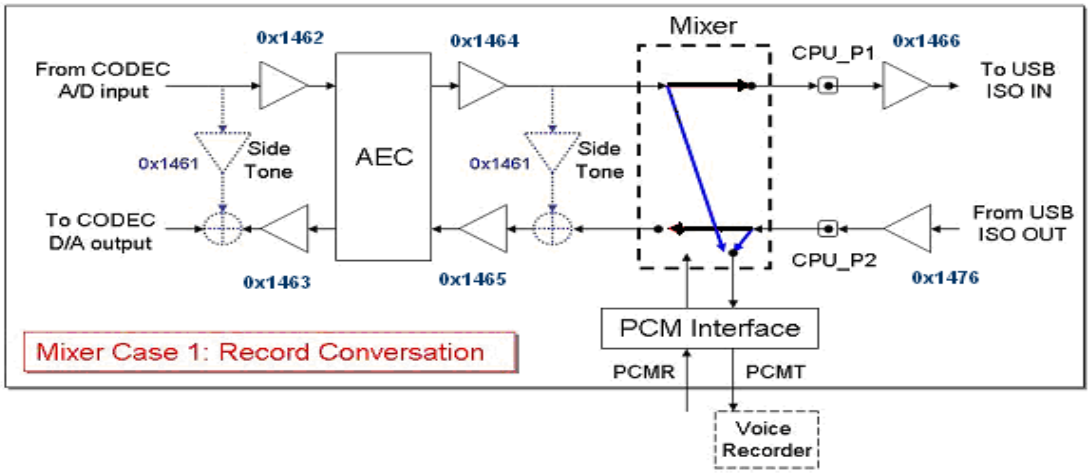
Figure 7 Mixer Examples with Registers Setting

Case 0: Default



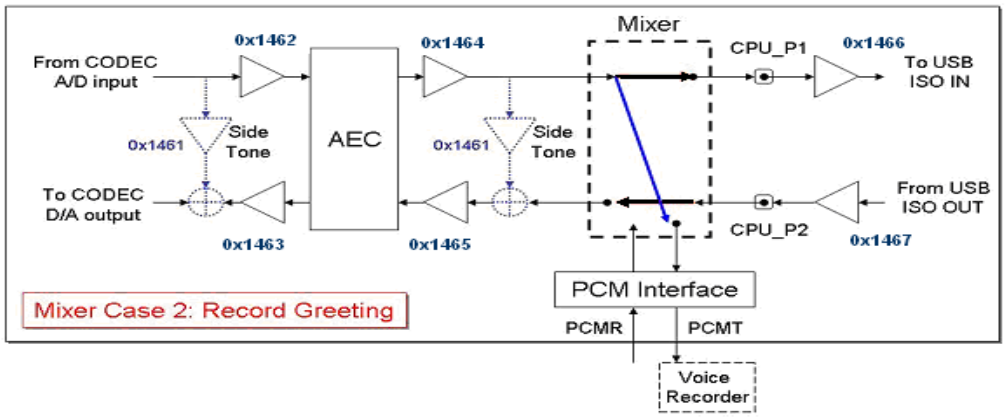
Register Setting:
0x1460 = 0x80 (Enable Gain Stage, Link CODEC_USB)
0x1470 = 0x00 (Disable PCM)

Case 1: Record Conversation



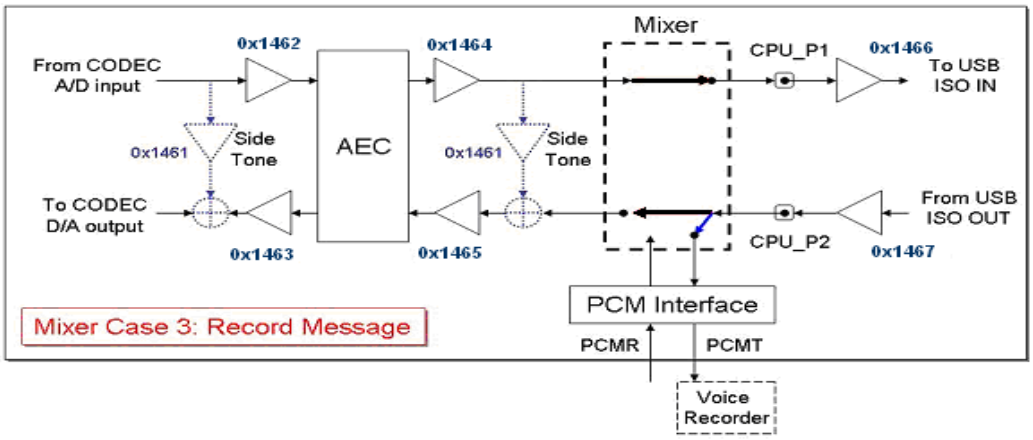
Registe. Setting:
0x1460 = 0x83 (Enable Gain Stage, Link All)
0x1470 = 0x80 (Enable PCM)
0x1474 = 0x02 (Mute PCM_RX)

Case 2: Record Greeting



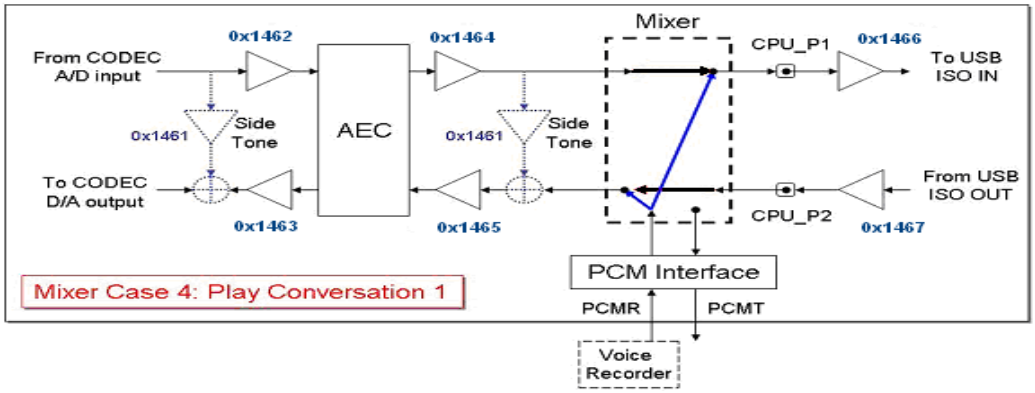
Register Setting:
0x1460 = 0x80 (Enable Gain Stage, Link CODEC_USB)
0x1470 = 0x80 (Enable PCM)
0x1474 = 0x02 (Mute PCM_RX)

Case 3: Record Message



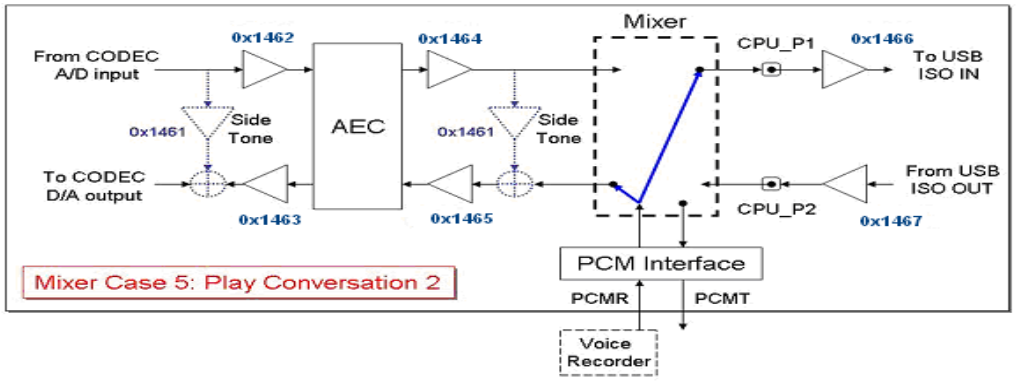
Register Setting:
0x1460 = 0xF0 (Enable Gain Stage, Link CODEC_USB, Record_USB)
0x1470 = 0x80 (Enable PCM)
0x1474 = 0x02 (Mute PCM_RX)

Case 4: Play conversation 1



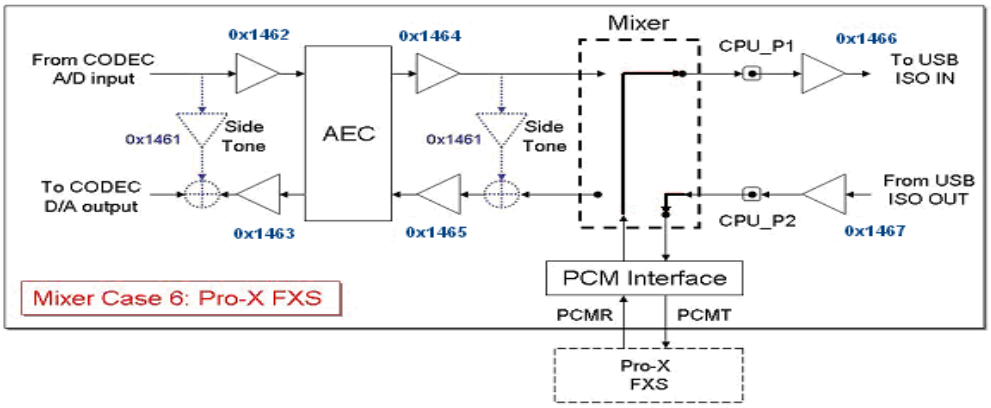
Register Setting:
0x1460 = 0x83 (Enable Gain Stage, Link All)
0x1470 = 0x80 (Enable PCM)
0x1474 = 0x04 (Mute PCM_TX)

Case 5: Play Conversation 2



Register Setting:
0x1460 = 0x83 (Enable Gain Stage, Link All)
0x1470 = 0x80 (Enable PCM)
0x1474 = 0x04 (Mute PCM_TX)
0x1464 = 0x40 (Mute CODEC A/D IN)
0x1467 = 0x40 (Mute USB ISO OUT)

Case 6: Pro-X FXS



Register Setting:
0x1460 = 0x81 (Enable Gain Stage, Link PCM_USB)
0x1470 = 0x80 (Enable PCM)
0x1465 = 0x40 (Mute CODEC D/A OUT)

12.6 I2S Register Setting Example

The following example will generate I2S interface format from the W681308 PCM interface.

I2S for 48KHz Sampling Rate(SR) with 16bits LPCM :

0x1470 = 85	
0x1470 [2:0]	101 = BCLK Rate Select. SR x 32 bits = 48K x 32 = 1.536MHz (L, R channels are 16 bits format)
0x1470 [4:3]	00 = FST Location, Frame Sync is occurred before the MSB of the PCM data.
0x1470 [7]	1 = Enable PCM Interface
0x1472	F0 = For long frame
0x1474	40 = PCM bit clock inverse enable

13. Audio Codec Interface

13.1 Overview

The audio CODEC interface allows the USB Audio Controller Device to be connected to one or more of the following:

- 16 bit internal linear PCM CODEC and Echo Cancellation block.
- 8/16/48 KHz CODEC sampling rate
- An I2S interface to and from the on chip linear CODEC.
- A PCM interface to connect to a external Nuvoton ProX SLIC/CODEC

The audio data is flowing between USB interface and CODEC through 2 segmented FIFOs that allow MCU processing of audio data.

13.2 Audio CODEC Signal Path

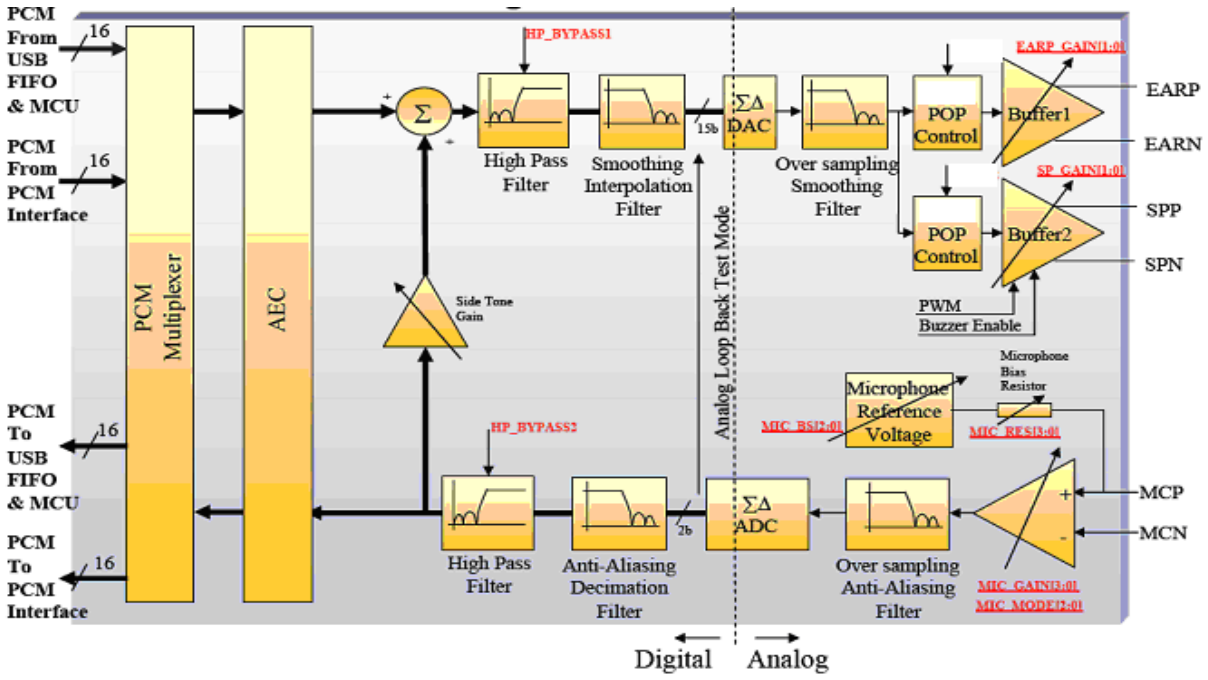


Figure 8 W681308 CODEC Signal Path Control

Transmit Path Operation

The microphone is biased through pins MCP by an internal programmable voltage reference and programmable resistor. The microphone ac signal is gained up by the input amplifier and filtered to prevent aliasing at the input of the sigma delta ADC. The sigma delta ADC converts the signal in a 2 bit digital representation, which is decimated and low pass filtered to the base band sampling rate of 8kHz to 48kHz. A high pass filter can be enabled in the transmit path.

The signal from the digital receive input is filtered through the acoustic echo cancellation filter and subtracted from the high pass filter output. The acoustic echo cancellation is only active in speaker phone operation with 8 kHz sampling. The result is then passed to the AGC with programmable time, release time and enable signal. The output of the AGC can be passed either to the PCM interface, the USB/MCU or both (recording a conversation).

Receive Path Operation

The PCM input can be obtained through a multiplexer from the PCM interface or the USB FIFO/MCU. The digital signal can then be gained or attenuated through a programmable digital gain stage. Then, the side tone from the transmit side is added through a programmable side tone gain stage. The side tone is disabled when the speakerphone is active.

The digital signal is then passed through a high pass filter with programmable enable. The output of the high pass filter goes through the interpolation smoothing filter, which produces a 4 bit binary to 15 bit thermometer digital representation for the sigma delta DAC. The output of the DAC goes through an analog smoothing filter. The output of the smoothing filter can be hooked up to the speaker phone speaker driver, the earphone speaker driver or both.

A programmable attenuation switch is used to switch between the earphone driver and the speaker phone driver. At power up of the analog section, the slow ramp on pin VREF1 is used to control the ramp up of the speaker and earphone driver in order to avoid 'POP' sounds. During operation, the user should lower the volume of the speaker using the software volume control settings, before switching the speaker and earphone driver in order to reduce the 'POP' sounds.;

Alternatively, a buzzer can be used on the speakerphone driver outputs, using a 200Hz- 32 kHz PWM signal. However, the speakerphone can not be used in that case.

Digital CODEC

The digital CODEC filter chain is so designed that it can handle 48K, 16K and 8K rate through its rate change filters.

13.3 Microphone Interface and Auxiliary Interface

W681308 integrates a fully programmable microphone interface. No external components other than the microphone are required to operate the circuit. The microphone interface can operate in three modes:

- Voltage gain mode
- Current gain mode
- Auxiliary input mode

For the Current gain mode an internal or external resistor can be selected to determine the gain. The Auxiliary input mode should be used with external resistors. However, an internal gain resistor can be selected. The interface modes above can be selected with register MIC_MODE [2:0] at address 0x1489.

- **Voltage Gain Mode**

The basic operation is shown below in
Figure 9. The microphone is connected to the pins MCP and RGND. It is important that the negative terminal of the microphone is routed separately to the RGND pin for 'pseudo differential' operation, reducing the background noise amplified by the microphone amplifier. This can be enforced in the PCB layout by placing a 0 Ohm resistor or a ferrite bead. The pin MCO is connected to the output of the microphone amplifier and can be used for monitoring the AC level. The voltage gain is set by register MIC_GAIN[7:4] at address 0x1489. This register provides a gain range from 14dB to 38dB. The gain is set by a ratio of internal resistors, providing accurate gain control. The pin MCP also supplies the bias reference for the microphone. The bias consists of a programmable resistor and a programmable voltage reference. The programmable resistor is set by register MIC_RES[7:4] at address 0x1488 and can be set to open and 670 Ohm to 10kOhm. The programmable voltage reference is set by register MIC_BIAS[2:0] at address 0x1488 and can be set from 1.22Volt to 2.74Volt.

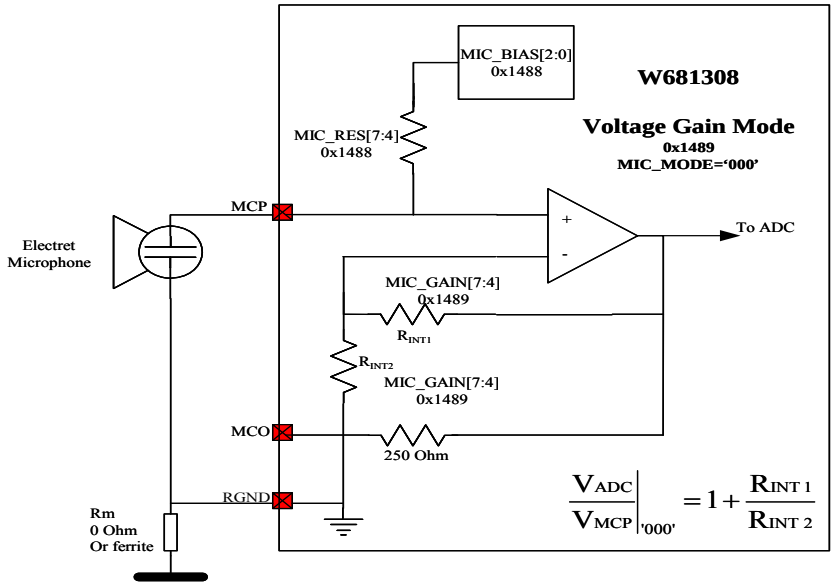


Figure 9 Microphone Voltage Gain Mode

- **Current Gain Mode**

For higher gain configurations, the current gain mode can be used as in Figure 10 below.

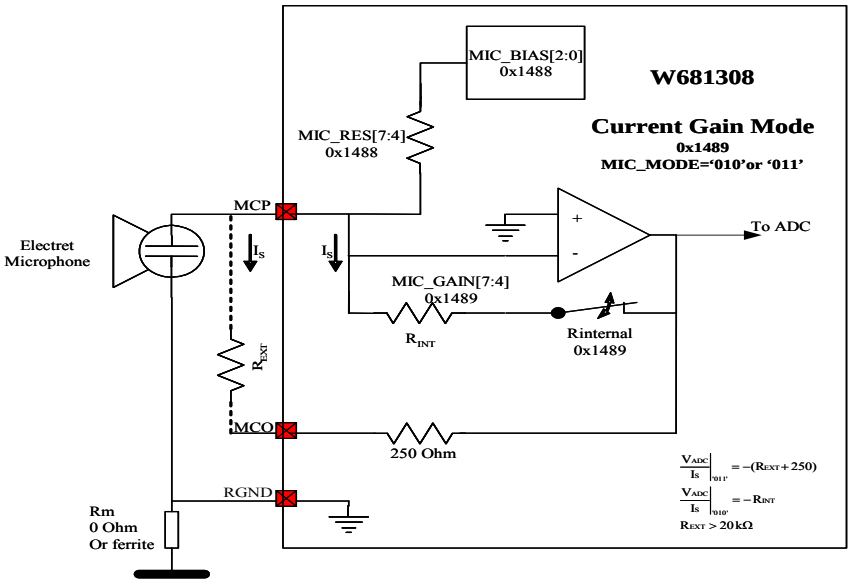


Figure 10 Microphone Current Gain Mode

The current gain mode uses the same programmable microphone bias voltage and resistor as the voltage gain mode. The gain is set by either the internal gain resistor or an external resistor, depending on the MIC_MODE setting. Since the current gain mode is using a single resistor, the gain accuracy is limited. However, large gain can be achieved. Note that a 250Ohm ESD protection resistor is connected to the MCO pin. This resistor should be considered when calculating the gain.

- **Auxiliary Input Mode**

For non-microphone applications one or more Auxiliary inputs can be connected to the MCP pin as shown in Figure 11 below. The MIC_RES register should be set to open in order to disconnect the microphone bias. For the gain setting it is advised to use external gain resistors only for optimal matching and accuracy. The 250Ohm ESD protection resistor should be considered again when calculating the gain. Note that for this mode the RGND pin is tied to the external supply ground. A clean ground reference should be used for this.

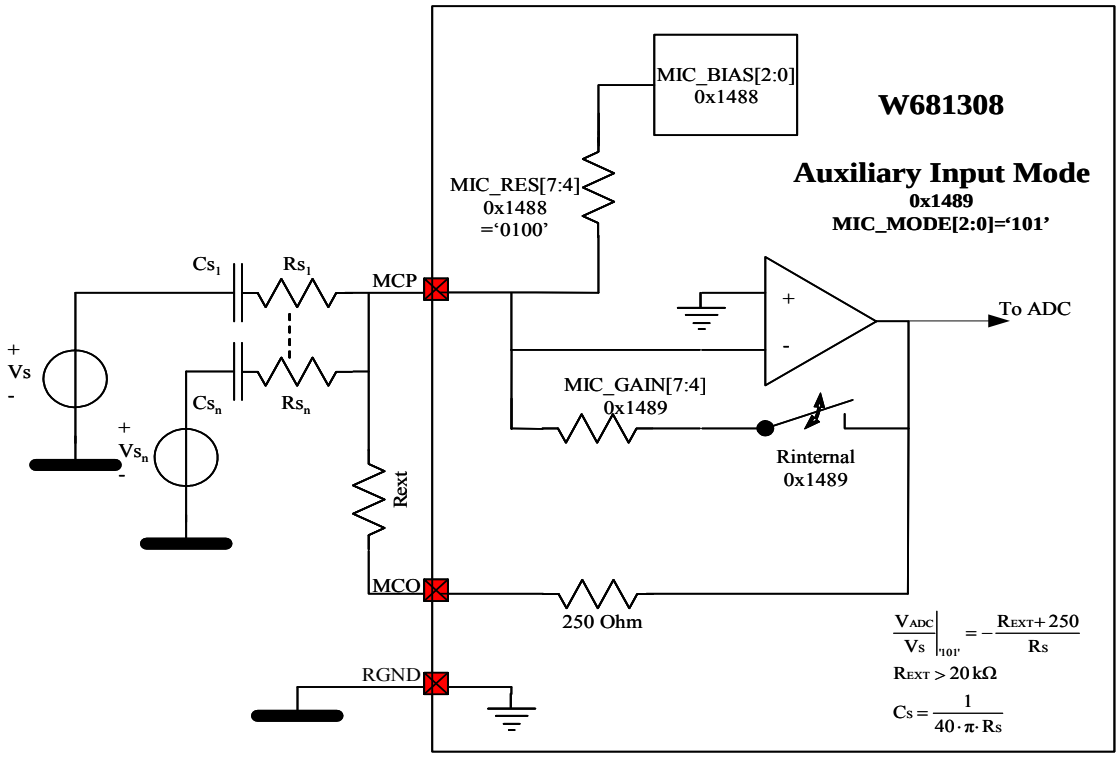


Figure 11 Microphone Auxiliary Input Mode

14. Serial Peripheral Interface

14.1 Overview

W681308 built in a serial peripheral interface (SPI) port which is a 4-pin (SCLK, CS, SDI, SDO) SPI Interface. This SPI interface makes W681308 an easy to control 4-pin SPI device including SPI data flash, SPI LCM, Nuvoton Pro-X SLIC CODEC etc. This device has various clock speed and data format by setting relative control registers. The SPI module can be operated at clock rates of up to MCU clock rate.

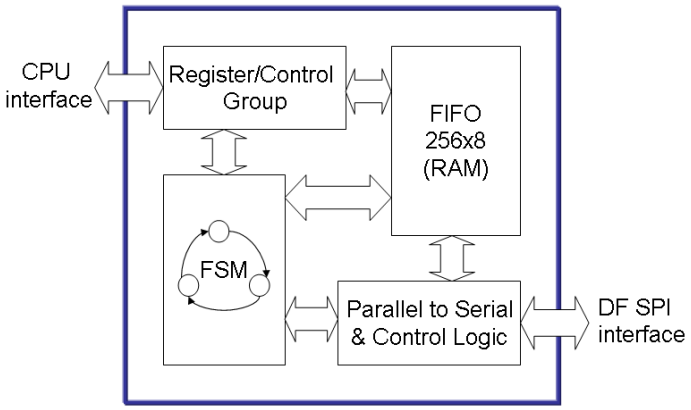


Figure 12 SPI Block Diagram

14.2 Data and Signal Format of SPI

There are 5 control bits (CSN_ADD, CSN_MORE, CK_MORE, CP and CI) to decide the SPI control signal format. Register 0x14AB has detail description of the control bits.

The packet and page data format is separated to 2 fields: Command field and the Data field. Command field (0 ~ 5 bytes) consists of control instruction/code and access address (TX only). Data field (0 ~ 256 bytes) consists of write and read data of serial data flash (TX/RX). All Command and Data bytes are send MSB first. Command and Data field length can be programmed in CMD_LEN (0x14A1[2:0]) and DATA_LEN (0x14A2[7:0]) register fields. It can be bypassed to write control bit CMD_BYPASS or disable the DATA_ENB. The max command field length is 5 bytes. The max data field length is 256 bytes in unidirectional mode, and 128 bytes in bidirectional mode. Thirteen examples are provided for reference.

14.3 FSM of SPI

There are 3 states in the SPI Finite State Machine (FSM) module. The initial state is IDLE when power on.

- **IDLE**

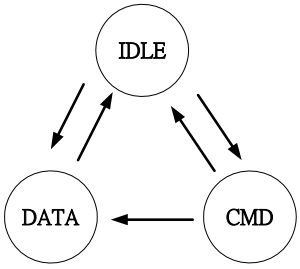
After enable the SPI function (write 0x14A0[7] =1), the FSM start to wait for MCU control (write 0x14A1) to change to next state. If the CMD BYPASS flag (0x14A1[5]) is true, the FSM will change to DATA state, then force control logic to shift in/out the data bytes sequentially. If the CMD BYPASS flag (0x14A1[5]) is false, the FSM will change to the CMD state, then force control logic to shift out the command bytes sequentially to external SPI device.

- **Command (CMD)**

After finished shift out the command bytes, the FSM will change to DATA state if the Data_enb (0x14A1[4]) is true, or run back to IDLE state if the Data_enb is false.

- **Data**

When FSM goes into Data state, the control logic start to shift out write data to external SPI device if SPI_RD (0x14A1[3]) is false, or shift in read data from external SPI device if SPI_RD (0x14A1[3]) is true. In bidirection mode, the control logic will ignore SPI_RD (0x14A1[3]) and start to shift in/out the read/write data from/to external SPI device. After finishing shift out/in the data bytes, the FSM will go back to IDLE state and wait for next transition.



14.4 FIFO and RAM of SPI

The SPI module takes up to 5 bytes Register to write the control command and takes the 256x8 bytes RAM to do the Read/Write access FIFO. In Bidirectional mode, the 256x8 bytes RAM will separate into two 128x8 bytes sections. One (ADDR: 0x00~7F) for keep the transmit data, and the other one (ADDR: 0x80~0xFF) for store the receive data. Once the Bidirectional mode is enabled, the SPI module will automatic put receive data from ADDR: 0x80 instead of the ADDR: 0x00 as in the unidirectional mode. It supports two memory access methods:

- **FIFO like method**

MCU always read/write the same register (0x14AC) with hardware control the memory read/write address, and increase the read/write pointer automatically after each read/write. The current write and read pointer can be read at register 0x14AE and 0x14AF.

- **Direct access method**

MCU can read/write any byte of the memory after setting the read (0x14AF)/write (0x14AE) pointer first.

14.5 Interrupt Sources

The SPI module supports two types of interrupt sources:

- **TX/RX finish interrupt**

When TX/RX byte counts (0x14AD) = DATA_LEN.

- **Middle flag interrupt**

When TX/RX byte counts (0x14AD) = 16 * INTR_CNT (0x14A3[7:4]).

For any other options, refer to the description of the specific registers in W681308 Design Guide.

15. Nuvoton 2-Wire Serial Bus

15.1 Overview

Nuvoton 2-wire serial bus (W2S) is a simple bi-directional 2-wire bus for efficient inter-IC control. This design is for W2S master use only, and governed by the MCU. The W2S is used to both read/write EEPROM and to control various device included I2C interface. The W2S controller is equipped with 35 bytes FIFO performing formatting and de-formatting. The MCU can simply fill up the FIFO contents which consists of target device ID, high/low address (depend on the device format); for reading, just set read enable, for writing, keep writing data to FIFO then set write enable to launch transmission. The W2S controller supports 3 types of page writing, 8, 16 and 32 bytes. The W2S controller is designed to support maximum of 32 bytes per page. The FIFO depth can support 3 header bytes (one device ID, two address) and 32 bytes data. It has various bus speed configurations to support wide range of EEPROM bus speed.

16. ICE Function By JTAG STD. IEEE 1149.1

16.1 Overview

The W681308 MCU on-chip debugger function follows the JTAG standard. It provides 8 sets of breakpoints. There is no watchpoint. There are five JTAG-style scan chains within the 8051 and peripheral logic, which enable embedded ICE logic. The 5 JTAG interface pins TCK (JTAG test clock input), TMS (JTAG test mode select), TDI (JTAG test data input), TDO (JTAG test data output) and nTRST (JTAG TAG controller reset) are needed to enable the operation. The JTAG interface pins are multiplexed with other function pins.

16.2 Scan Chains and JTAG Interface

There are five JTAG-style scan chains within the TB51 core and peripheral logic interface. These enable debugging operation and configuration of Embedded-ICE logic. An external pull low signal on nTRST will reset TAP controller or MCU power-on reset will trigger TAP controller reset once.

16.3 Pin Description

Table 11 JTAG Pin Description

Pin Name	Type	Function
TCK	IN	JTAG Test clock with internal pull-up.
TMS	IN	JTAG Test-Mode Select with internal pull-up.
TDI	IN	JTAG Test Data Input with internal pull-up. TDI is latched on a rising edge of TCK.
TDO	OUT	JTAG Test Data Output. Data is shifted out on TDO at the rising edge of TCK. TDO output is a tri-state driver with internal weakly pull-low resister.
nTRST	IN	JTAG TAP controller reset input with internal pull-up.

16.4 Reset Behavior

TB51 will start to execute internal code after power on reset. If host JTAG ICE connects with TB51, the host ICE can send command to control the TB51.

Reset type	Functional description
Power On Reset	1. Reset MCU 2. Reset JTAG. TAP controller will stay in Test-Logic Reset State. 3. Execution starts from address 0000 after reset.
Reset by RESET pin or WDT RESET (including set Reset out and Reset in SC0)	1. Reset Chip. 2. Do not reset JTAG. TAP controller stays in the original state. 3. If the original TAP controller state is in run mode, chip reset 4. If the original TAP controller state is in Halt mode. No any state changed
nTRST Low	1. No effect on MCU. 2. Reset JTAG. TAP controller will stay in Test-Logic Reset state.

17. Ring Tone (PWM) Generator

17.1 Overview

The ring tone or PWM can generate dual frequency tones through on chip speaker driver. There are two tone signals can be mixed to the speakerphone driver output. This subsection describes the Ring Tone Generator with the PWM (Pulse Width Modulation) format.

Ring tone generator (PWM) specification:

- Tone Channel Number = 2
- Tone Volume Step = 32
- Tone Frequency Range = 91Hz~23KHz

$$Frequency = \frac{12M}{16 \times N \times 32}\ Hz \qquad N = 1 \sim 256$$

The tone frequency/volume control signal path is shown as Figure 13.

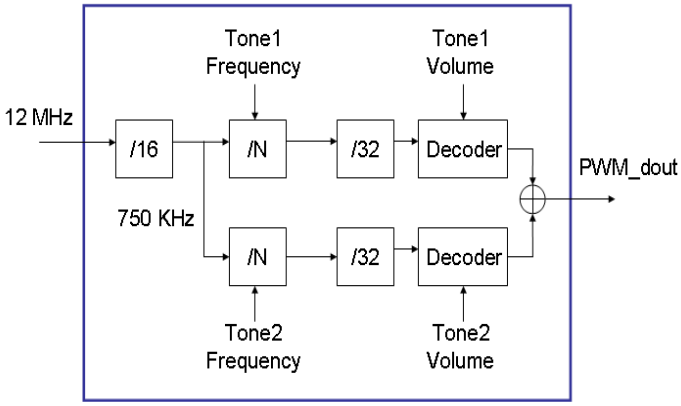


Figure 13 Ring Tone Generator Block

18. FULL/HALF DUPLEX ACOUSTIC ECHO CANCELLATION(AEC)

The AEC unit removes the echo signal caused by the speaker and room reflections.

18.1 Function Control Registers

Figure 14 illustrates the block diagram of the Full/Half Acoustics Echo Cancellation

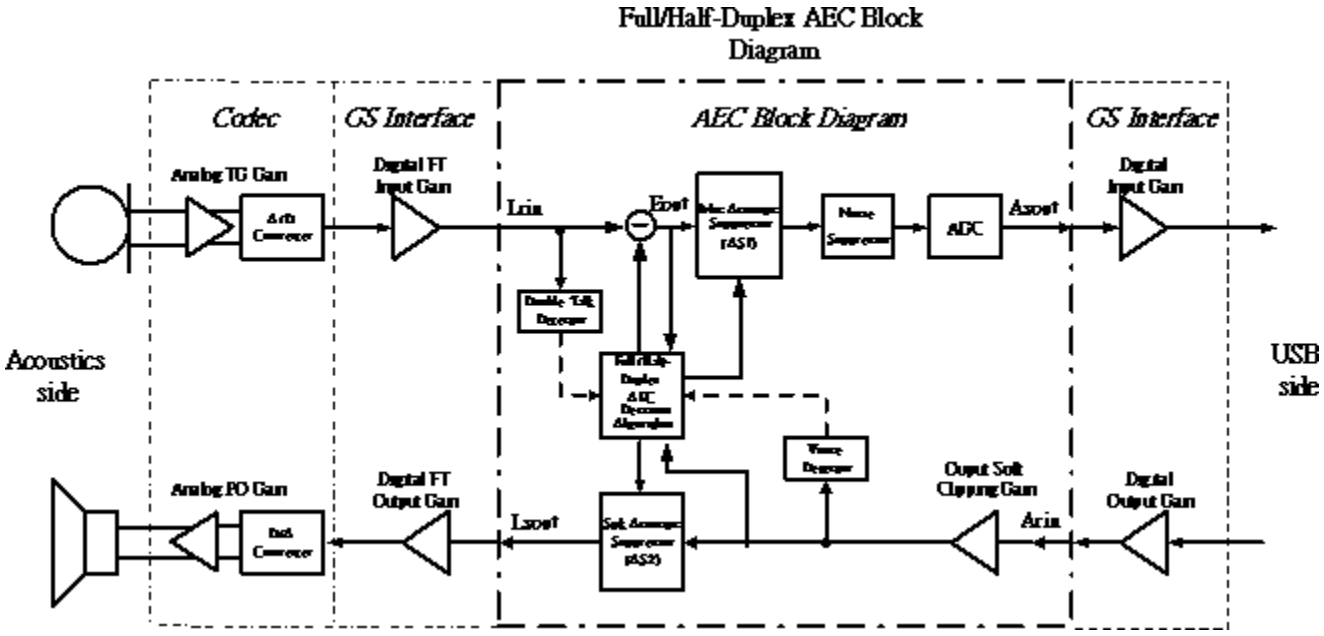


Figure 14 Signal flow through Acoustic Echo Cancellation in the speech processor

19. USB Device Controller And Transceiver

19.1 Overview

The W681308 includes a full function USB 2.0 Full Speed controller. It supports USB 2.0 FS standard specification and standard USB audio device class and HID device class in Microsoft Windows environment. The USB core embeds one programmable 512x8 Bit RAM to store descriptor. In the setting, the USB core includes five interfaces and 6 endpoints to handle above applications.

19.2 Functional Description

The USB function block diagram is shown below:

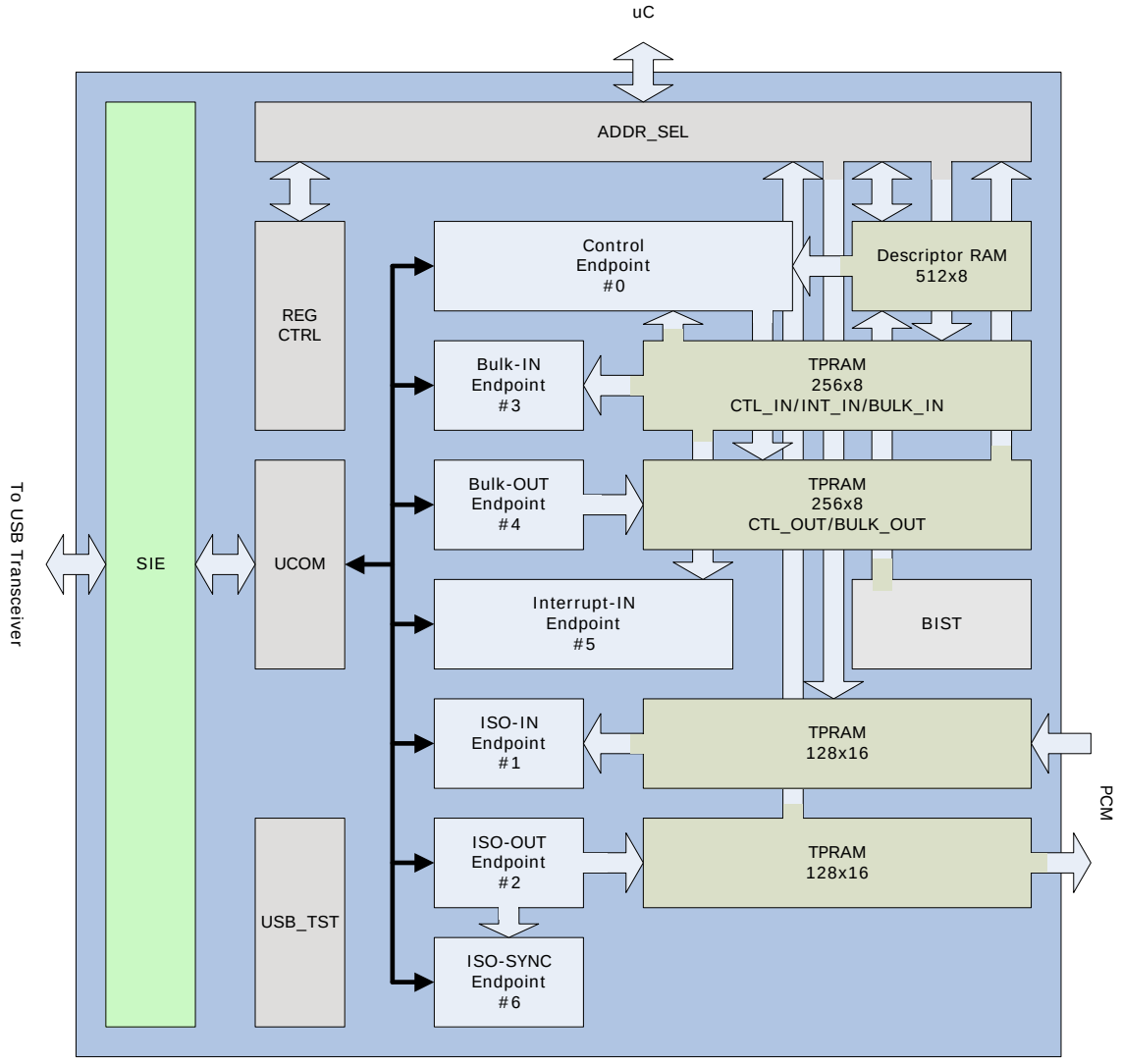


Figure 15 USB Function Block Diagram

The USB module supports all transfer types (Control, Bulk In, Bulk Out, Interrupt In, Isochronous In, Isochronous Out and ISO-SYNC) in USB 1.1 spec and W681308 USB embeds 6 Endpoints include Control Endpoint 0. The default descriptors are stored in the programmable 512x8 Bit RAM. The SIE module is for handle USB series-interface-engine functions. UCOM

module is a bridge to communicate SIE and all transfer type modules. Register Control module is for handle MCU read/write and data signals of W681308 USB registers. Gain Stage residing out off USB module is required for adjusts gain of PCM data in audio volume control application. USB test module connects many internal signals to test pins for help monitor them from outside.

The features of USB interface are:

- USB Specification version 2.0 Full Speed(FS) 12Mbps compliant
- Audio Class Interface and Command support (Volume Control, Mute Control, Sampling Rate selection)
- HID Class Interface and Command support (Set/Get Report)
- Programmable pull-up resistor to connect/disconnect 1.5Kohm on D+ bus
- Support five interfaces and 6 endpoints: Control, Isochronous IN/OUT, Bulk IN/OUT, and Interrupt IN.
- Ping-Pong FIFO control for Bulk IN/Bulk OUT transfer to increase data transmission efficiency.
- Provide three bytes Isochronous SYNC to synchronize Isochronous OUT with PC audio data stream and improve voice quality.

19.2.1 Endpoints

The definitions of embedded endpoints are:

Address	Type	Direction	maximum Packet Size (Bytes)	Memory Type
0	Control	IN/OUT	64	64x8 TPRAM
1	ISO	IN	256	128x16 TPRAM
2	ISO	OUT	256	128x16 TPRAM
3	Bulk	IN	128	128 x 8 TPRAM
4	Bulk	OUT	128	128 x 8 TPRAM
5	Interrupt	IN	64	64x8 TPRAM
6*	ISO	IN	3	Registers

Table 12 W681308 USB Endpoint Definitions

NOTE: TPRAM - Dual Ports RAM

19.2.2 Descriptor RAM

The referenced descriptors are stored in the 512x8 Bit RAM, programmed by MCU. The address mapping and bank definition of this RAM are shown in 18-2.

Address	Function	Size
0x2000~0x2011	Device Descriptor	18 Bytes
0x2012~0x217F	Configuration Descriptor Interface Descriptor Endpoint Descriptor Audio Class Descriptor HID Descriptor	366 Bytes
0x2140~0x214F	String Descriptor Index 0	16 Bytes
0x2150~0x215F	String Descriptor Index 1	16 Bytes
0x2160~0x216F	String Descriptor Index 2	16 Bytes
0x2170~0x217F	String Descriptor Index 3	16 Bytes
0x2180~0x21FF	Report Descriptor	128 Bytes

Table 13 USB Descriptor RAM Definitions

20. Electrical Characteristics

20.1 Absolute Maximum Ratings

CONDITION	VALUE	UNIT
Junction temperature	150	^{0}C
Storage temperature range	-65 to +150	^{0}C
Lead temperature (soldering – 10 seconds)	300	^{0}C
LQFP-48 Thermal Resistance, typical	76	C/W
Voltage applied to any pin	(V_{SS} - 0.3) to (V_{DD} + 0.3)	V
Input current applied to any digital input pin	+/- 10	mA
ESD (Human Body Model)	2000	V
V_{DD} - V_{SS}	-0.5 to +3.63	V
V_{DDL} - V_{SS}	-0.5 to + 1.98	V
Power Dissipation	0.5	Watt

NOTE: Stresses above the value listed may cause permanent damage to the device. Exposure to absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

20.2 Recommended Operating Conditions

CONDITION	VALUE	UNIT
Commercial operating temperature	0 to +70	^{0}C
Industrial operating temperature	-40 to +85	^{0}C
Supply voltage (V_{DD}) using external regulator	+3.13 to +3.47	V
Supply voltage (V_{DDUSB}) using internal regulator and external transistors	+4.4 to + 5.25	V
Ground voltage (V_{SS})	0	V

20.3 DC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VIL	Input Low Voltage	-0.3		0.8	V
VIH	Input High Voltage	2		3.6	V
VT	Threshold point	1.32	1.41	1.49	V
VT+	Schmitt trigger. Low to High threshold point	1.49	1.54	1.58	V
VT-	Schmitt trigger. high to low threshold point	1.24	1.29	1.34	V
II	Input leakage current @*VI*=3.3V or 0V			± 10	μA
IOZ	Tri-state output leakage current @*VO*=3.3V or 0V			± 10	μA
RPU	Pull-up resistor	38	54	83	K
RPD	Pull-down resistor	25	49	110	K
VOL	Output low voltage @*IOL* (min)			0.4	V
VOH	Output high voltage @*IOH* (min)	2.4			
IOL	Low level output current @*VOL*=0.4V 2 mA	2.2	3.7	5.3	mA
	Low level output current @*VOL*=0.4V 16 mA	19.6	29.8	39.0	mA
IOH	High level output current @*VOH*=2.4V 2 mA	3.2	6.4	10.6	mA
	High level output current @*VOH*=2.4V 16 mA	23.1	46.8	77.8	mA

20.4 Analog Transmission Characteristics

AVDD=3.13V – 3.47V; V_{SS}=0V; T_A=-40°C to +85°C; All ADC tests using Auxiliary input mode @ 0dB gain

PARAMETER	SYMBOL	CONDITION	TYP	TRANSMIT (ADC)		RECEIVE (DAC)		UNIT
				MIN	MAX	MIN	MAX	
Full Scale Level	T_{XmaX}	ADC (single ended) DAC (differential)	1.218 2.436	--- ---	--- ---	--- ---	--- ---	V_{PK} V_{PK}
Absolute Gain	G_{ABS}	-3dBFS @ 1020 Hz, AVDD =3.3V; T_A=+25°C;	0	-0.40	+0.40	-0.40	+0.40	dB
Absolute Gain variation with Temperature	G_{ABST}	T_A=0°C to T_A=+70°C T_A=-40°C to T_A=+85°C -3dBFS	0	-0.10 -0.20	+0.10 +0.20	-0.10 -0.20	+0.10 +0.20	dB
Absolute Gain variation with Supply Voltage	G_{ABSS}	AVDD=3.13V – 3.47V; -3dBFS @ 1020 Hz; T_A=+25°C	0	-0.10	+0.10	-0.10	+0.10	dB

20.5 Analog Distortion and Noise Parameters

All ADC tests using Auxiliary input mode @ 0dB gain

20.5.1 8kHz sampling

AVDD=3.13V – 3.47V; V_{SS}=0V; T_A=-40°C to +85°C; 8kHz sampling

PARAMETER	SYMBOL	CONDITION	TRANSMIT (ADC)			RECEIVE (DAC)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Signal to Noise Ratio	SNR	Idle channel A-weighted	80	94	--	80	88	--	dB
Total Harmonic Distortion	THD3	-3dBFS @ 1020 Hz, 32Ohm speaker load	--	-77	-67	--	-77	-67	dB
Total Harmonic Distortion	THD8	-3dBFS @ 1020 Hz, 8Ohm speaker load	--	-77	-67	--	-70	-60	dB
Total Harmonic Distortion	THD4	-6dBFS @ 1020 Hz, 4Ohm speaker load	--	-79	-69	--	-65	-55	dB
Frequency Response	Frl	-3dB Low pass cut-off		3.36			3.36		kHz
Power Supply Rejection	$PSRR_A$	V_{DDUSB}; 35mVrms DC to 3.4 kHz A-weighted	70	88	---	70	85	---	dB

20.5.2 16kHz sampling

AVDD=3.13V – 3.47V; V_{SS}=0V; T_A=-40°C to +85°C; 16kHz sampling

PARAMETER	SYMBOL	CONDITION	TRANSMIT (ADC)			RECEIVE (DAC)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Signal to Noise Ratio	SNR	Idle channel A-weighted	80	93	--	80	86	--	dB
Total Harmonic Distortion	THD3	-3dBFS @ 1020 Hz, 32Ohm speaker load	--	-76	-66	--	-78	-68	dB
Total Harmonic Distortion	THD8	-3dBFS @ 1020 Hz, 8Ohm speaker load	--	-76	-66	--	-70	-60	dB
Total Harmonic Distortion	THD4	-6dBFS @ 1020 Hz, 4Ohm speaker load	--	-79	-69	--	-65	-55	dB
Frequency Response	Frl	-3dB Low pass cut-off		6.73			6.73		kHz
Power Supply Rejection	$PSRR_A$	V_{DDUSB}; 35mVrms DC to 6.8 kHz A-weighted	70	89	---	70	85	---	dB

20.5.3 48kHz sampling

AVDD=3.13V – 3.47V; V_{SS}=0V; T_A=-40°C to +85°C; 48kHz sampling

PARAMETER	SYMBOL	CONDITION	TRANSMIT (ADC)			RECEIVE (DAC)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Signal to Noise Ratio	SNR	Idle channel A-weighted	80	92	--	80	85	--	dB
Total Harmonic Distortion	THD3	-3dBFS @ 1020 Hz, 32Ohm speaker load	--	-77	-67	--	-76	-66	dB
Total Harmonic Distortion	THD8	-3dBFS @ 1020 Hz, 8Ohm speaker load	--	-77	-67	--	-69	-59	dB
Total Harmonic Distortion	THD4	-6dBFS @ 1020 Hz, 4Ohm speaker load	--	-78	-68	--	-65	-55	dB
Frequency Response	Frl	-3dB Low pass cut-off		20.2			20.2		kHz
Power Supply Rejection	$PSRR_A$	V_{DDUSB}; 35mVrms DC to 6.8 kHz A-weighted	70	88	---	66	76	---	dB

20.6 Programmable Output Linear Regulator

T_A=-40°C to +85°C; Using discrete components per application diagram;

PARAMETER	SYMBOL	CONDITION	MIN (2)	TYP (1)	MAX (2)	UNIT
Recommended USB Supply Voltage	V_{DDUSB}	Low Power Mode (100mA) High Power Mode (500mA)	4.4 4.75	5 5	5.25 5.25	V V
Regulated Supply Voltage	V_{DD}	No Load, Normal Operation	3.13	3.3	3.47	V
Total Suspend Mode Current	I_{SP}	Suspend Mode Including USB pull-up and discrete regulator	--	463	--	uA
Operating Supply Current	I_{VDD}	No Load, Normal Operation	--	38	--	mA
Voltage Drop	$V_{DROP0.5}$	V_{DDUSB} =5V, load=500mA	--	0.006	--	V
Voltage Drop	V_{DROP1}	V_{DDUSB} =5V, load=1A	--	0.06	--	V

NOTE 1: Typical values: TA = 25°C
NOTE 2: All min/max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested

20.7 USB PHY Electronic Characteristics (25°C, DVDD= 3.3V, VDDL =1.8V)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage for USB Output Stage	VDD_USB		3.1	3.3	3.5	V
Input Voltage Range for USB_DP/DN	USB_DP USB_DN		0		3.5	V
Input High	V_{IH}		2.0			V
Input Low	V_{IL}				0.8	V
Differential Input Sensitivity	V_{DI}		0.2			V
Differential Common-mode Range	V_{CM}		0.8	---	2.5	V
Single-end Receiver threshold	V_{SE}		0.8		2.0	V
Output Low	V_{OL}				0.3	V
Output High	V_{OH}		2.8			V
Output signal cross Voltage	V_{CRV}		1.3		2.0	V
Pull-up Resistor	R_{UP}		1.3	1.61	1.9	KΩ
Driver Output Resistance	Z_{DRV}		8		19	Ω
Transceiver Capacitance	C_{IN}				20	pF
Driver Rise Time	T_R	C_L = 50pF Rs=25 Ohms C_{Edge}=30pF	4	8	20	ns
Driver Fall Time	T_F		4	8	20	ns
Rise and Fall Time matching	T_{LRLF}	$T_{LRLF} = T_{LR}/T_{LF}$	90	100	110	%
VDD_USB Supply Current * (exclude internal pull high resistor)	I_{USB}	Standby			100	nA
		Input Mode			2	mA
		Output Mode			2	mA

20.8 USB PLL Electronic Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operation Voltage	V_{PLL}		3.13	3.3	3.47	V
Input Clock Frequency Range	F_{IN}			12		MHz
PLL Output Frequency	F_{OUT}			48		MHz
VCO Frequency	F_{VCO}		---	48	---	MHz
Ouput Duty Cycle			46	56	66	%
PLL Short-Term Peak To Peak Output Jitter	T_{JITTER}			7		ps
PLL Lock In Time	T_{READY}			25		us

21. Typical Application Reference Circuit

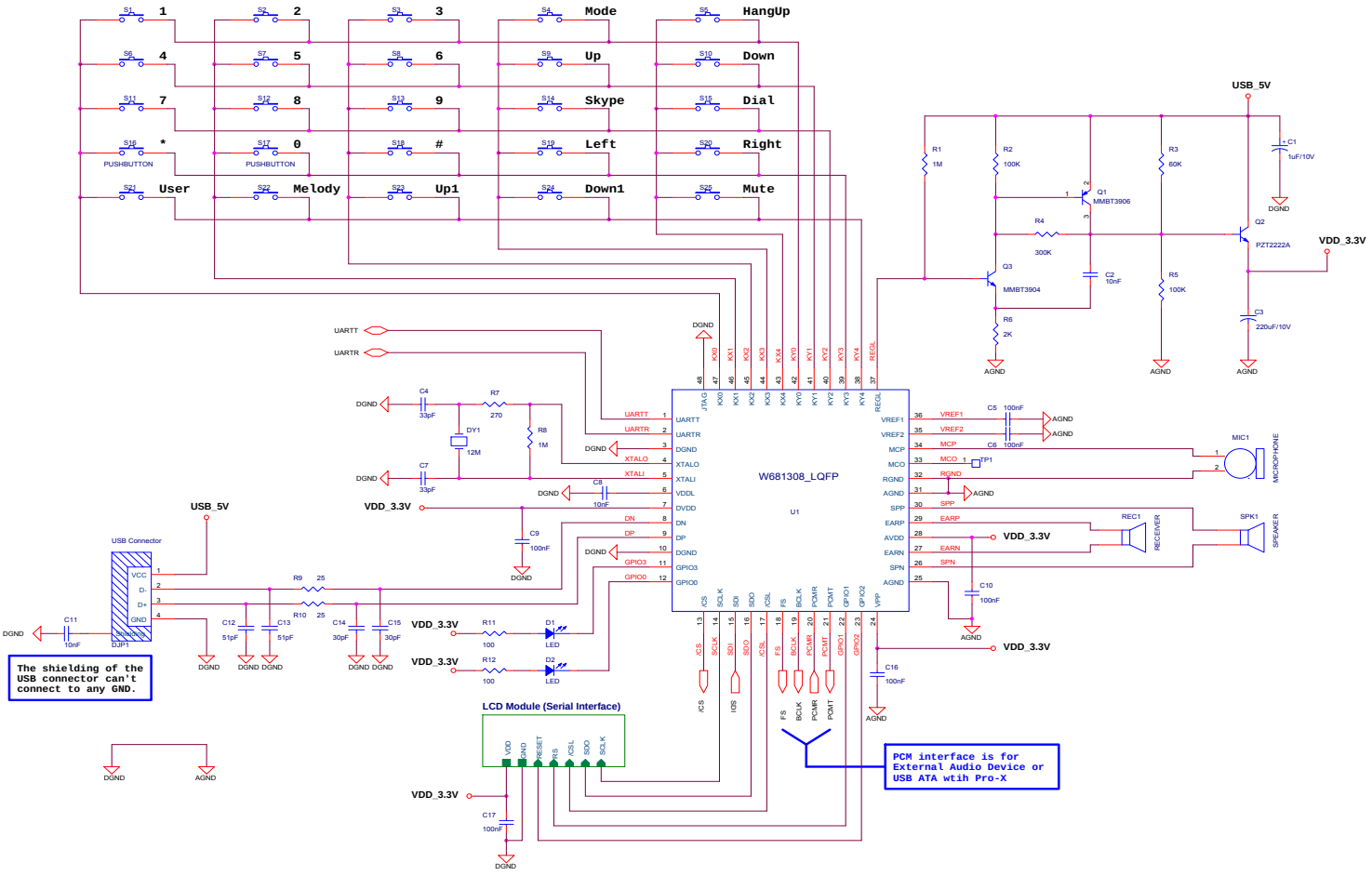


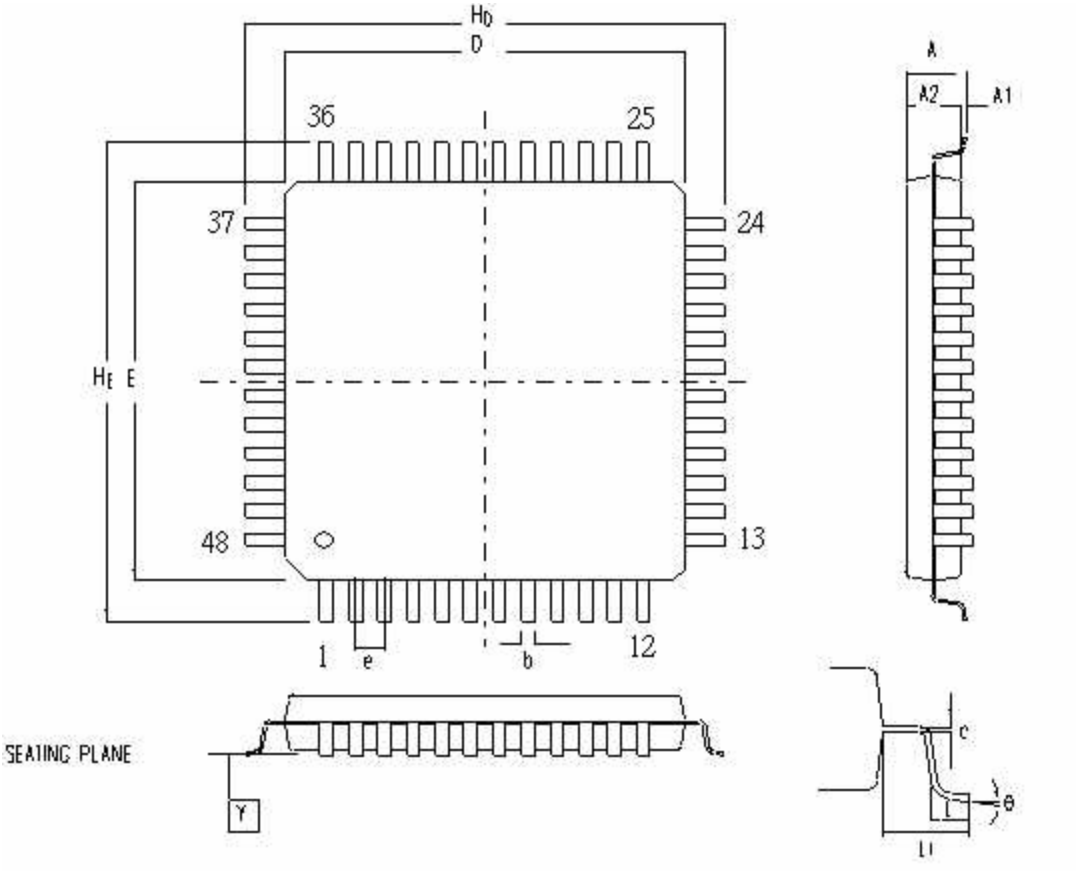
Figure 16 W681308 Reference Design Application Circuit

21.1 USB VoIP speaker phone application

The application diagram illustrated that the W681308 is a SOC with very low BOM system design. Externally it supports a variety interfaces such as keypad, LCM, SLIC, SPI flash/EEPROM, Microphone and speakers directly. External 12M Crystal as well as a 5V to 3.3V linear regulator is required. Ring tone download and playback is through the same Audio DAC path with a switch for ringing and speech.

22. Package Dimensions

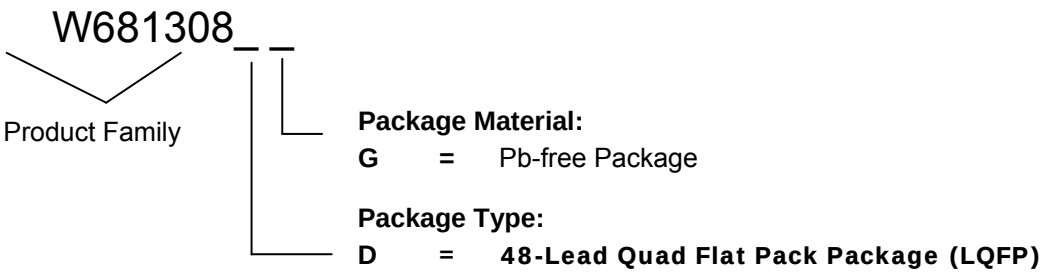
W681308DG is in 48 pin Low-profile Quad Flat Package (LQFP).



Symbol	In inch			In mm		
	min	nom	max	min	nom	max
A	-	-0.063	-	-	1.60	
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.008	0.010	0.15	0.20	0.20
c	0.004	0.005	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.025	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1		-	0.039	-	-	1.00
Y	-	-	0.004	-	-	0.10
θ	0’	-	7’	0’	-	7’

23. Ordering Information

Nuvoton Part Number Description



When ordering W681308series devices, please refer to the following part numbers:

Part Number	Temp Range (°C)	Package	Package Material
W681308DG	-40 to 85	48-LQFP	Pb-Free

24. Revision History

VERSION	DATE	PAGE	DESCRIPTION
V0 9	July, 2007		Preliminary Version
V1.0	August, 2007		Update Electrical Characteristics
V1.1	March, 2008		Update Speaker / Earphone attenuation switch
V1.2	March 2009		Format of the datasheet changed Logo update

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